

COMPAL CONFIDENTIAL

MODEL NAME : BAL20
PCB NO : DAZ1P600100
BOM P/N : 431A2K31L01

SKL-U+MEC1404 board
2016-06-21
REV : 1.0 (A00)

@ : Un-pop Component
UMA@/DIS@ : UMA & DIS Type
KBL@/SKL@ : CPU Type
EC@ : EC
JP@/PJP@ : JUMP

EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
CMC@ : XDP Component
CONN@ : Connector Component
TP_WAKE@/NTP_WAKE@ : TouchPad wake
KBBL@ : KB Backlight
3D@/3D@EMI@ : 3D Camera
@3D@ : 3D Camera Un-POP Component

M1_70R1@ : GPU R1
M1_70R3@ : GPU R3
2G@/2G_H@/2G_S@/2G_M@ : VRAM type
4G@/4G_H@/4G_S@/4G_M@ : VRAM type

zzz

PCB

DAZ1P600100

PCB@

PCB BAL20 LA-D801P LS-D801P/D802P/D803P

KBL R3

UC1

i7-R1

SA0000A344L

i7KBL2.7G_R3@

S IC FJ8067702739740 SR2ZV H0 2.7G A31!

UC1

i5-R1

SA0000A374L

i5KBL2.5G_R3@

S IC FJ8067702739739 SR2ZU H0 2.5G A31!

SKL R3

UC1

i7-R3

SA000092P3L

i7SKL2.5G_R3@

FJ8066201930408 SR2EZ D1 2.5G A31!

UC1


i5-R3

SA000092O3L

i5SKL2.3G_R3@

FJ8066201930409 SR2EY D1 2.3G A31!

Layout Dell logo



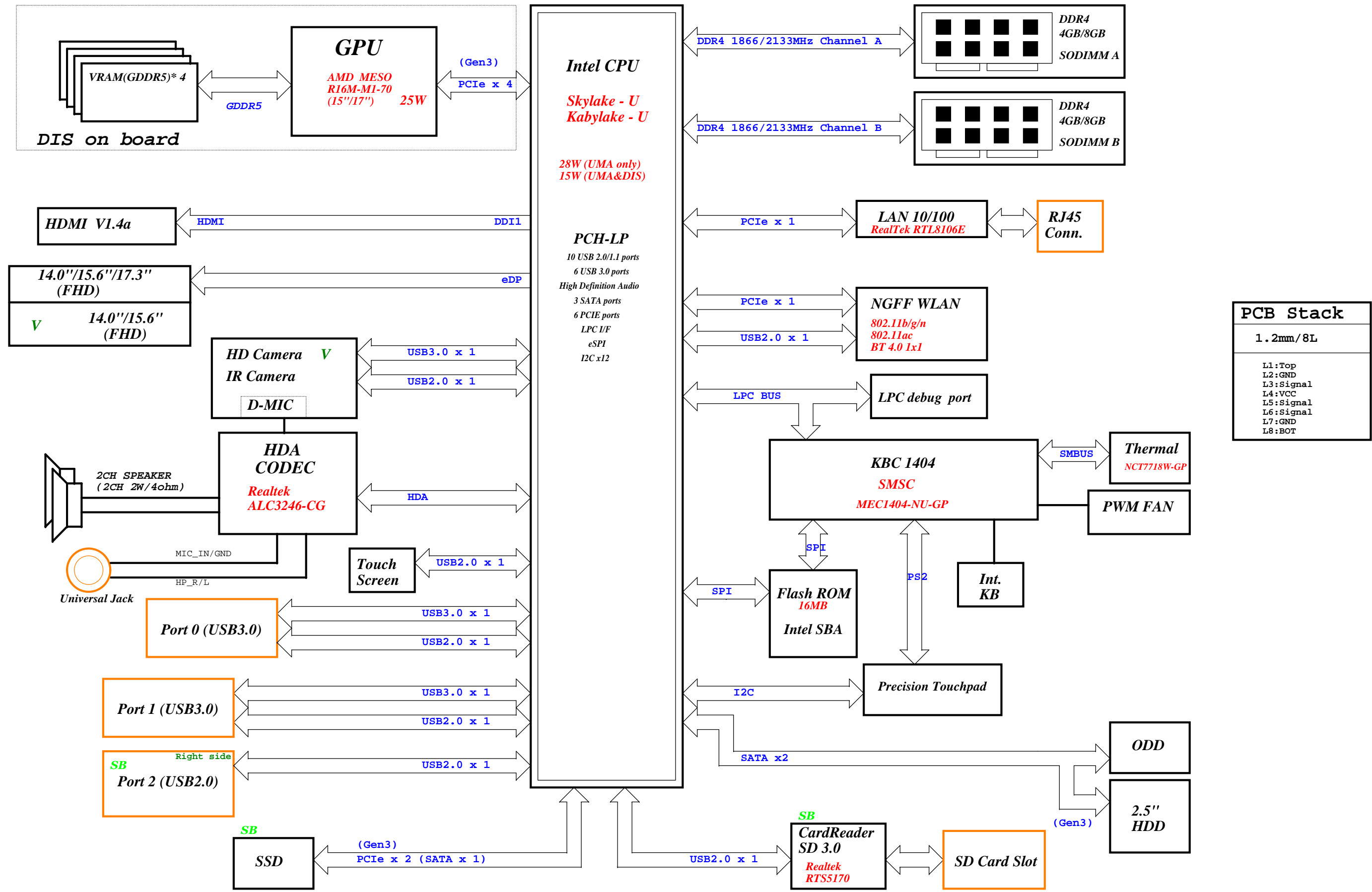
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Block Diagram



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF

USB PORT#	DESTINATION
1	USB3.0 Port1
2	USB3.0 Port2
3	IO/DB
4	N/A
5	CCD
6	Card Reader
7	Touch Screen
8	BT
9	N/A
10	N/A

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				USB3.0 Port1
USB3.0-2	SSIC-1			USB3.0 Port2
USB3.0-3	SSIC-2			3D Camera
USB3.0-4				N/A
USB3.0-5		PCIE-1		GPU
USB3.0-6		PCIE-2		GPU
		PCIE-3		GPU
		PCIE-4		GPU
		PCIE-5		WLAN
		PCIE-6		10/100M LAN
		PCIE-7	SATA-0	SATA HDD
		PCIE-8	SATA-1	SATA ODD
		PCIE-9		N/A
		PCIE-10		N/A
		PCIE-11	SATA-1*	N/A
		PCIE-12	SATA-2	N/A

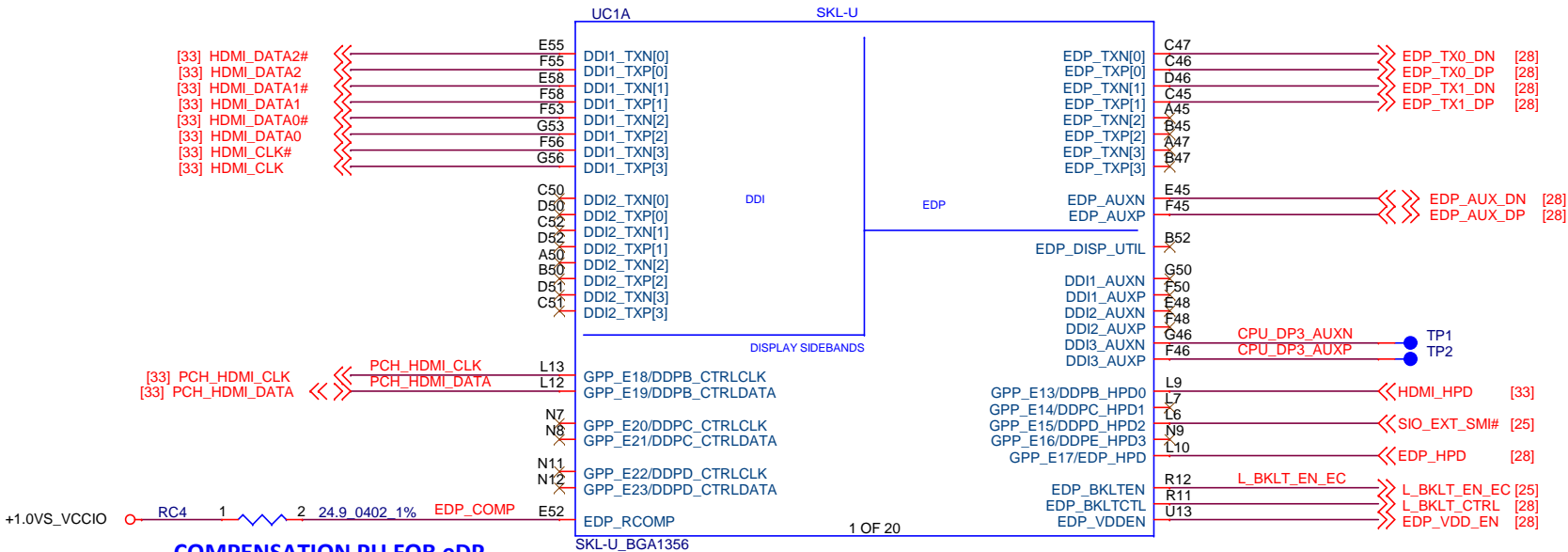
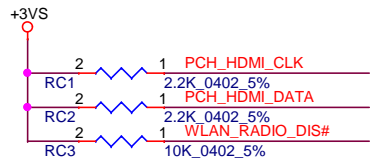
PM TABLE

power plane State	+RTC_CELL	B+	+1.0V_PRIM +1.0V_MPHYGT +1.8V_PRIM +3VALW +3VALW_PCH +3.3V_ALW_DSW +5VALW	+1.0V_VCCST +1.2V_DDR +2.5V_MEM	+1.0VS_VCCIO +1.0V_VCCSTG +VCC_GT +VCC_SA +VGA_CORE +VCC_CORE +0.6V_DDR_VTT
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
M3	ON	ON	ON	ON	OFF
S4&S5 / AC	ON	ON	ON	OFF	OFF
S4&S5 / AC doesn't exist	ON	ON	OFF	OFF	OFF
G3	ON	OFF	OFF	OFF	OFF

Board ID & Model ID table

Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10.0	3.000	EVT
2	100	13.7	2.902	DVT1
3	100	17.8	2.801	DVT2
4	100	22.1	2.703	
5	100	27.0	2.598	
6	100	32.4	2.492	
7	100	37.4	2.402	
8	100	49.9	2.201	Pilot
9	100	57.6	2.094	
10	100	64.9	2.001	
11	100	73.2	1.905	
12	100	82.5	1.808	
13	100	93.1	1.709	
14	100	107.0	1.594	
15	100	120.0	1.500	
16	100	137.0	1.392	
17	100	154.0	1.299	
18	100	200.0	1.100	
19	100	232.0	0.994	

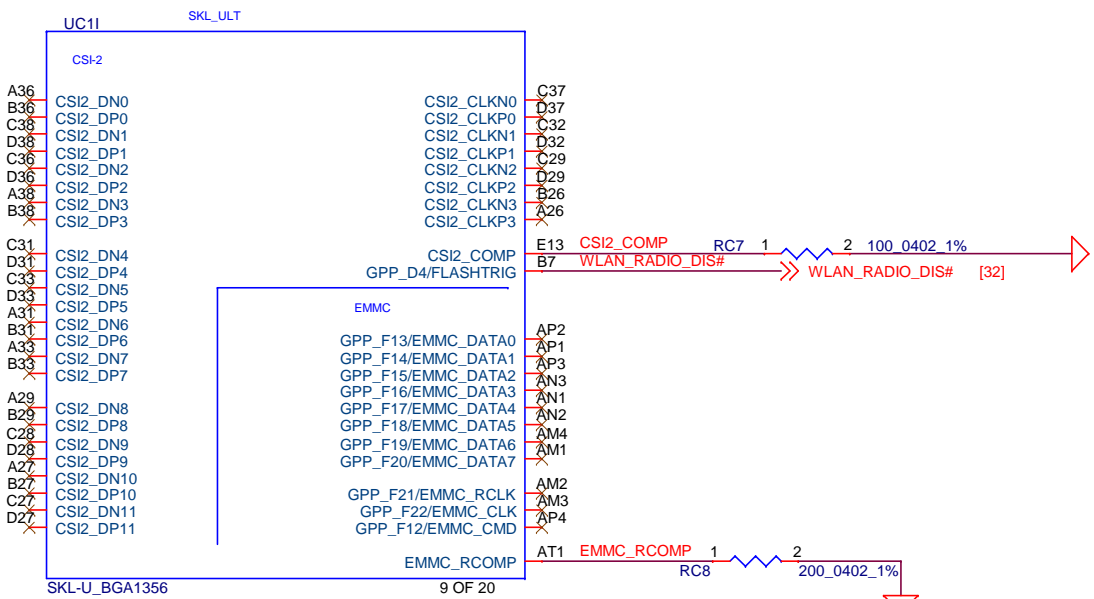
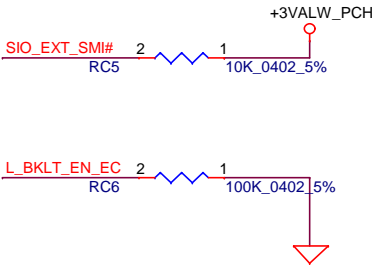




COMPENSATION PU FOR eDP

CAD Note:Min trace width=5 mils ,Spacing=25mil,
Max length=600 mils.

SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0



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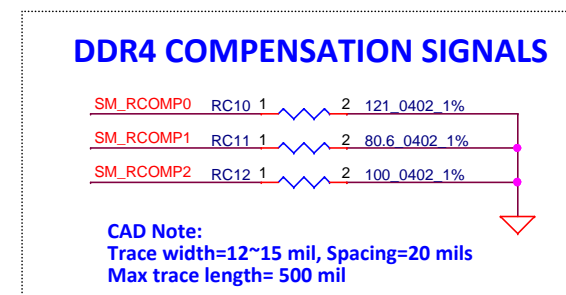
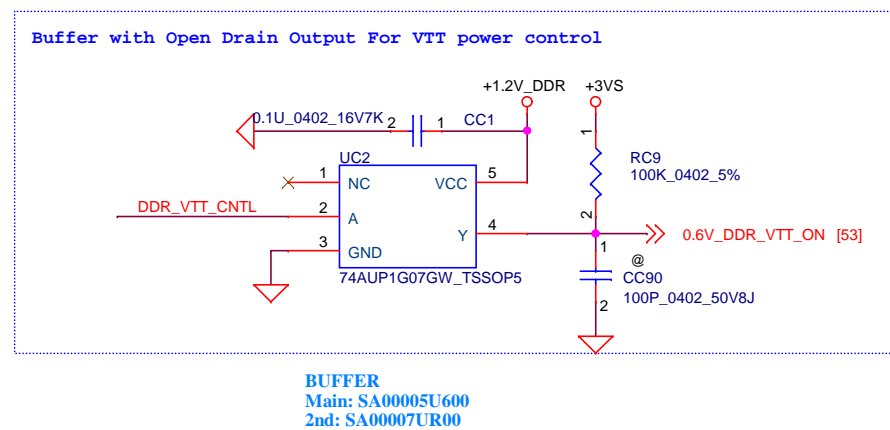
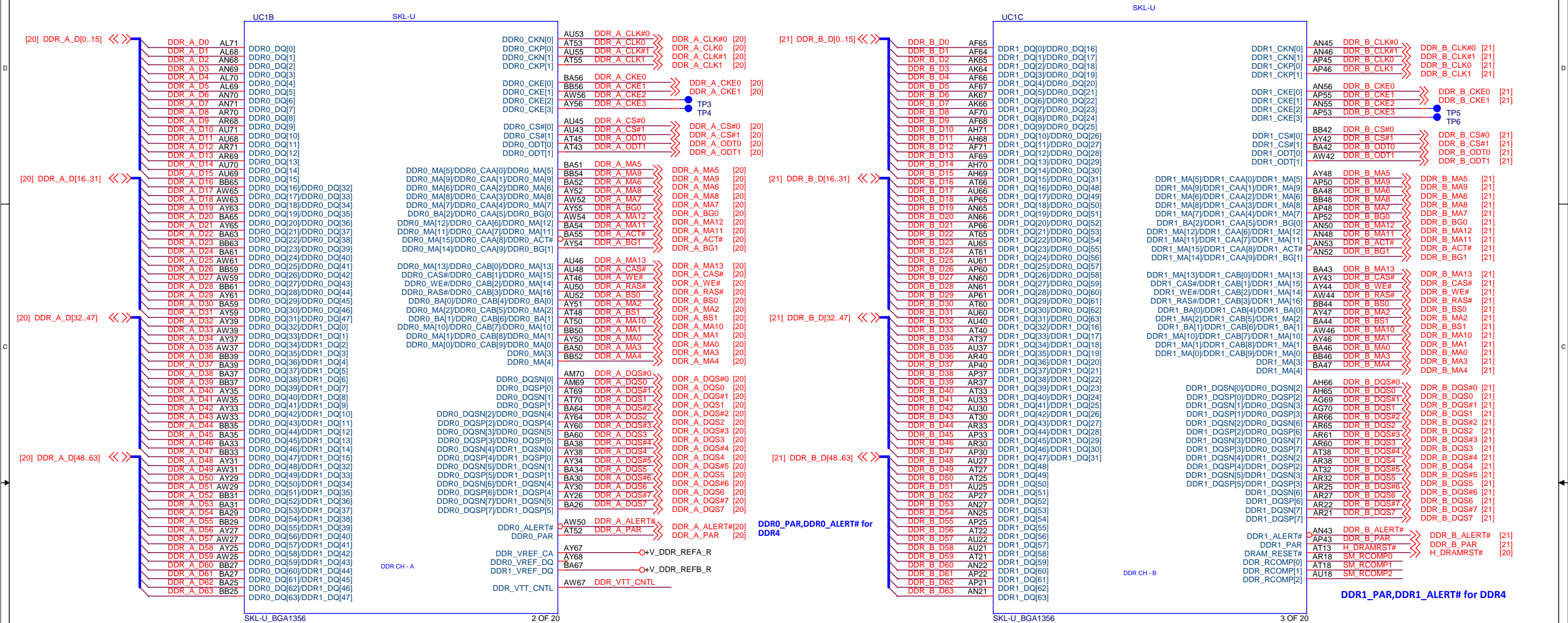
MCP(1/14)DDI,EDP,CSI2,EMMC

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DDR4 Interleaved Memory



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Size

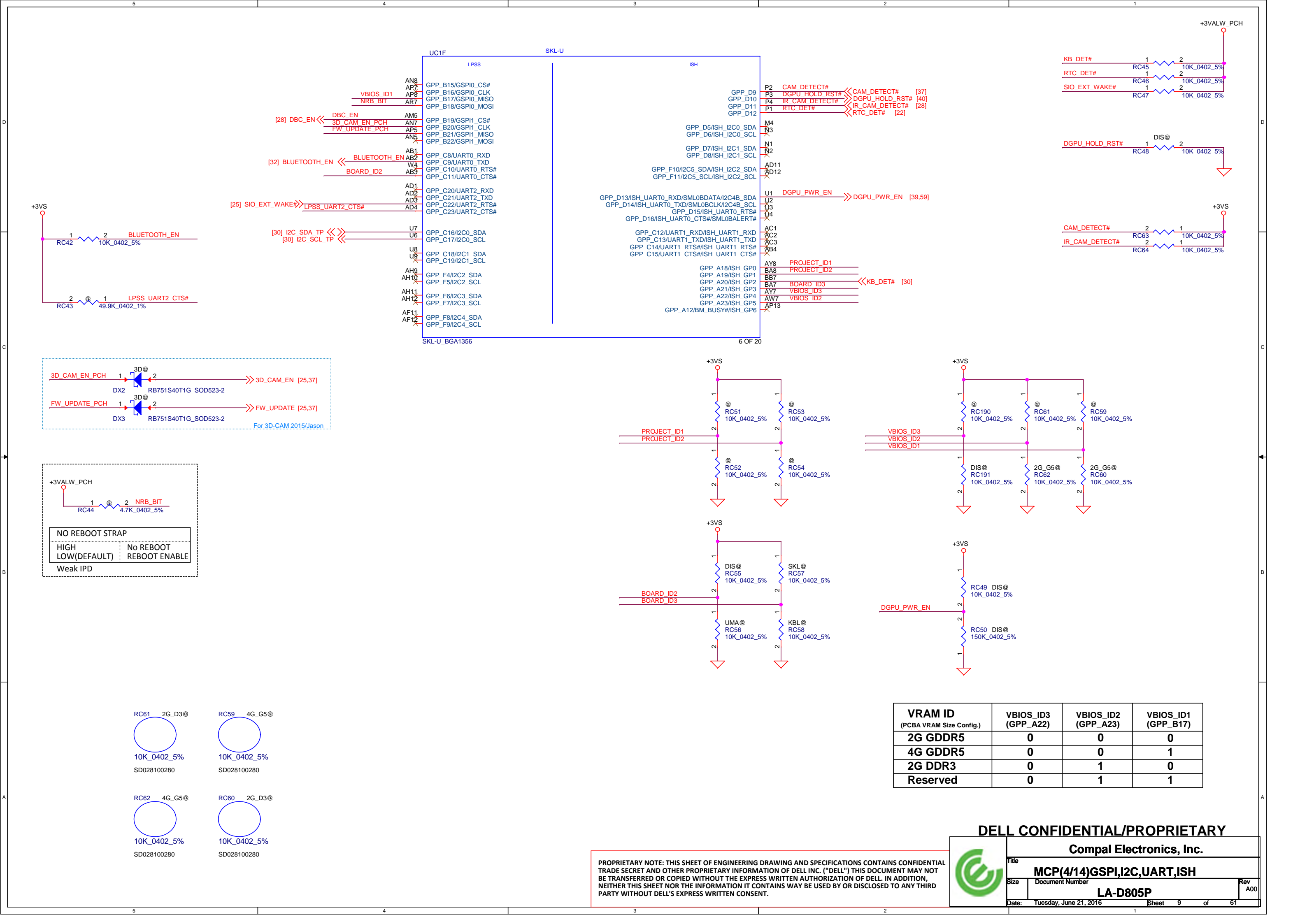
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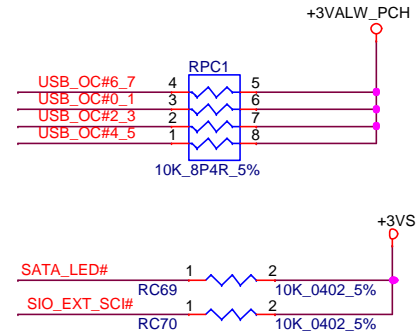
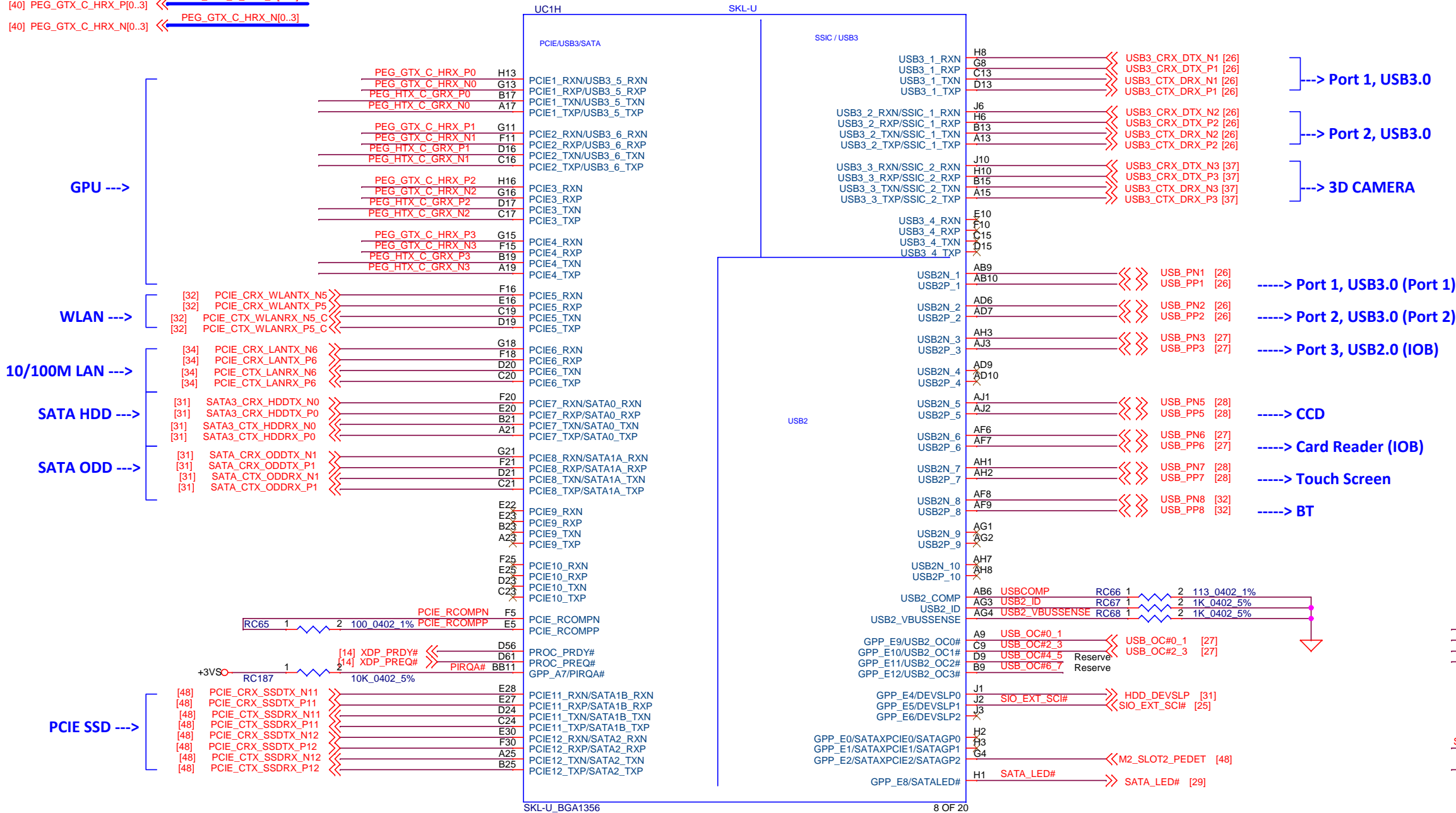
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[40] PEG_HTX_C_GRX_P[0..3] >> PEG_HTX_C_GRX_P[0..3]
[40] PEG_HTX_C_GRX_N[0..3] >> PEG_HTX_C_GRX_N[0..3]
[40] PEG_GTX_C_HRX_P[0..3] << PEG_GTX_C_HRX_P[0..3]
[40] PEG_GTX_C_HRX_N[0..3] << PEG_GTX_C_HRX_N[0..3]



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MCP(5/14)PCIE,USB,SATA

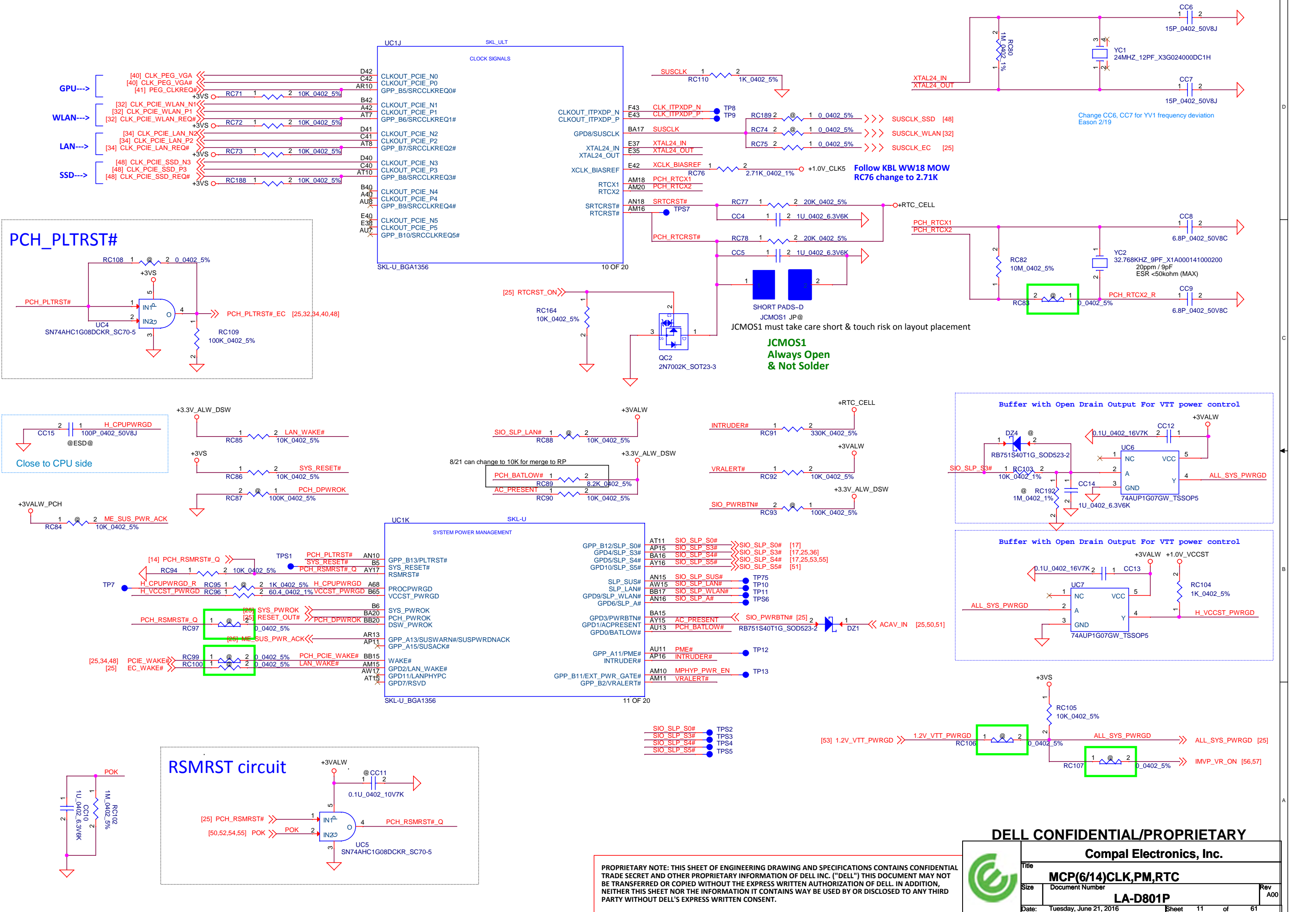
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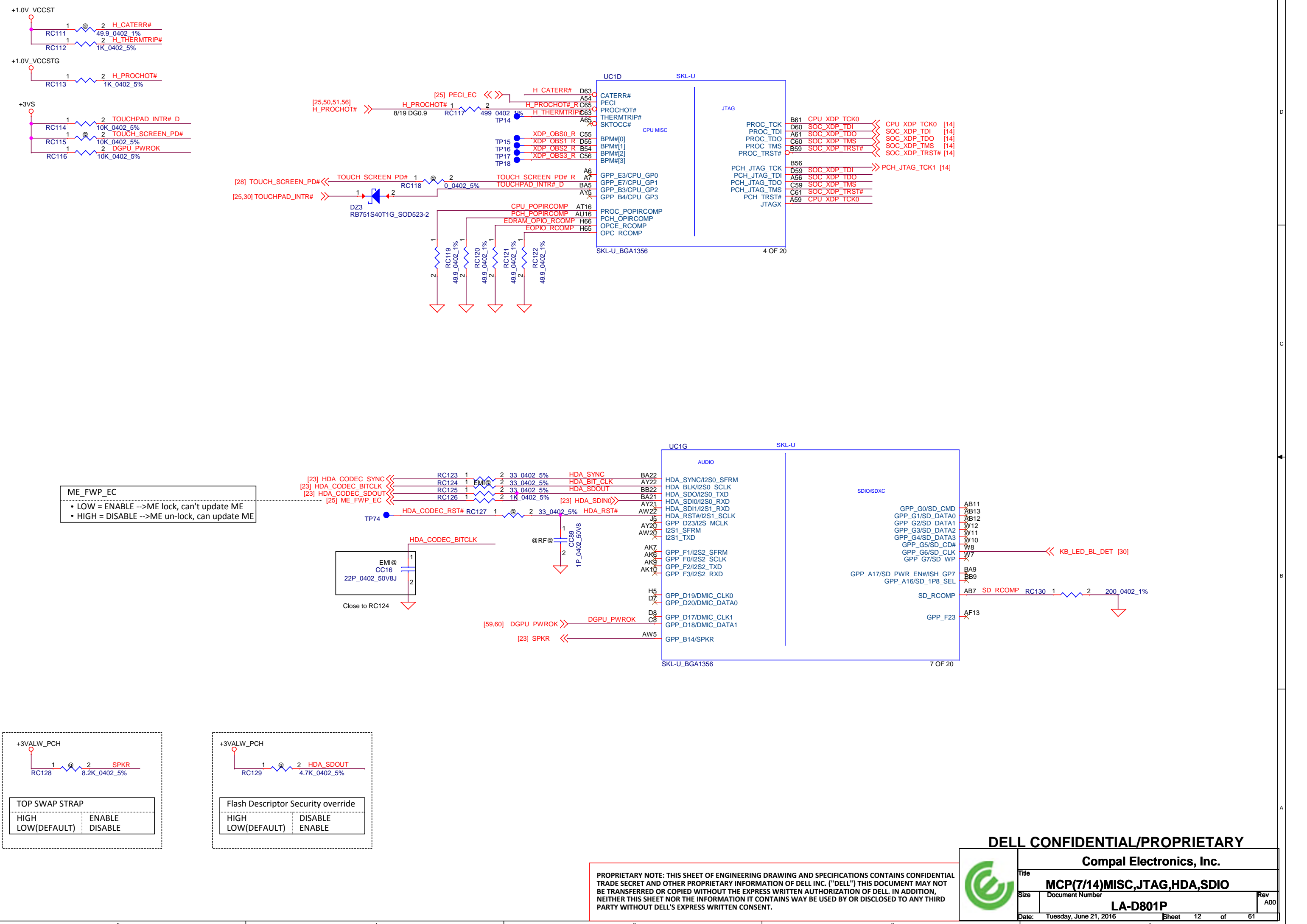
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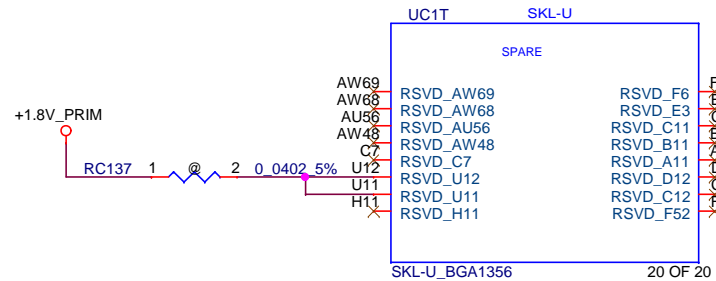
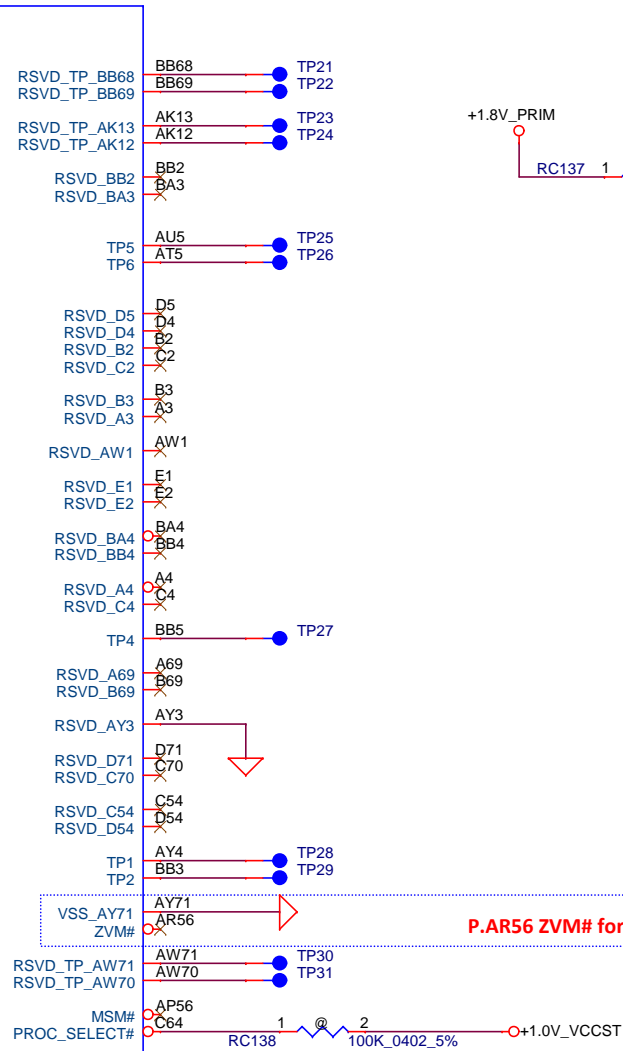
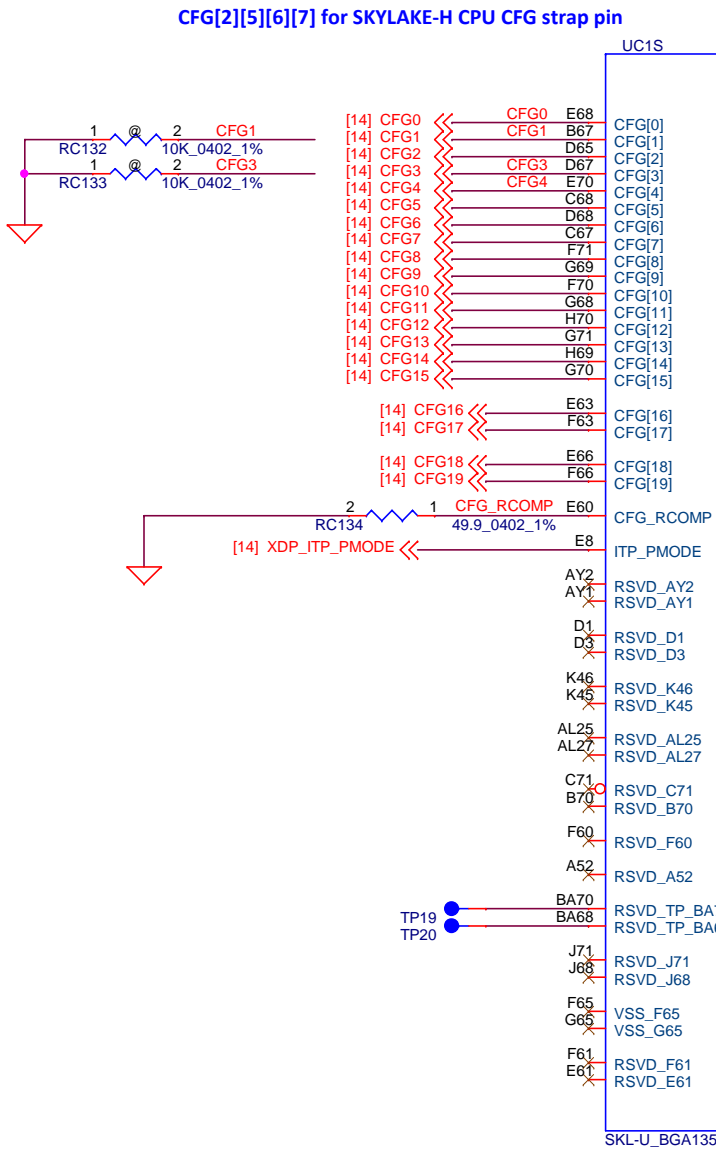
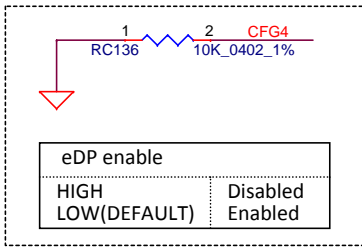
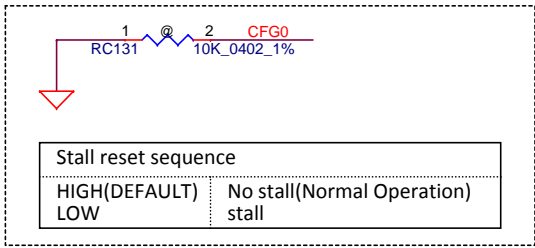
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Title MCP(7/14)MISC,JTAG,HDA,SDIO

Size Document Number LA-D801P

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Title

MCP(8/14)CFG,RSVD

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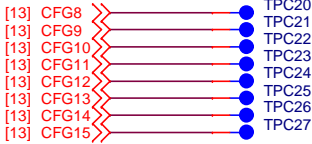
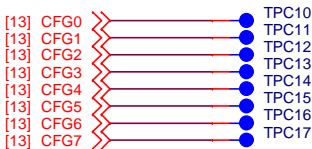
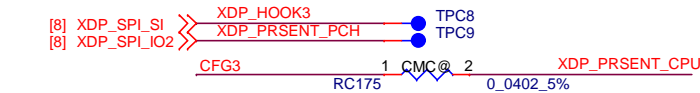
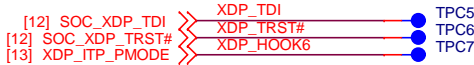
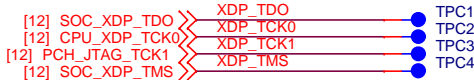
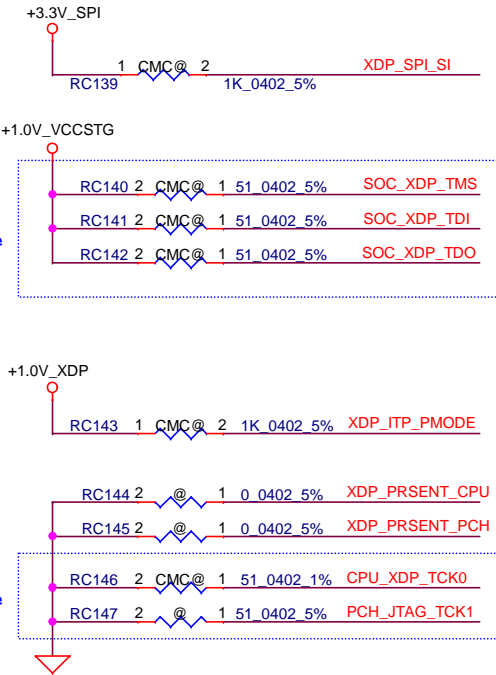
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Connector Less Routing Topology

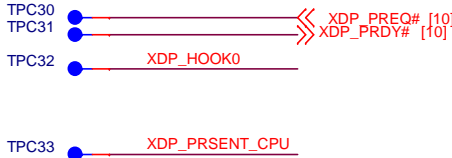
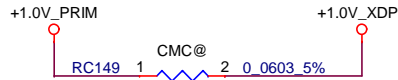
DCI Link
RC142 need POP
RC146 need POP

Place to CPU side

Place to CPU side



PRIMARY CMC CONN



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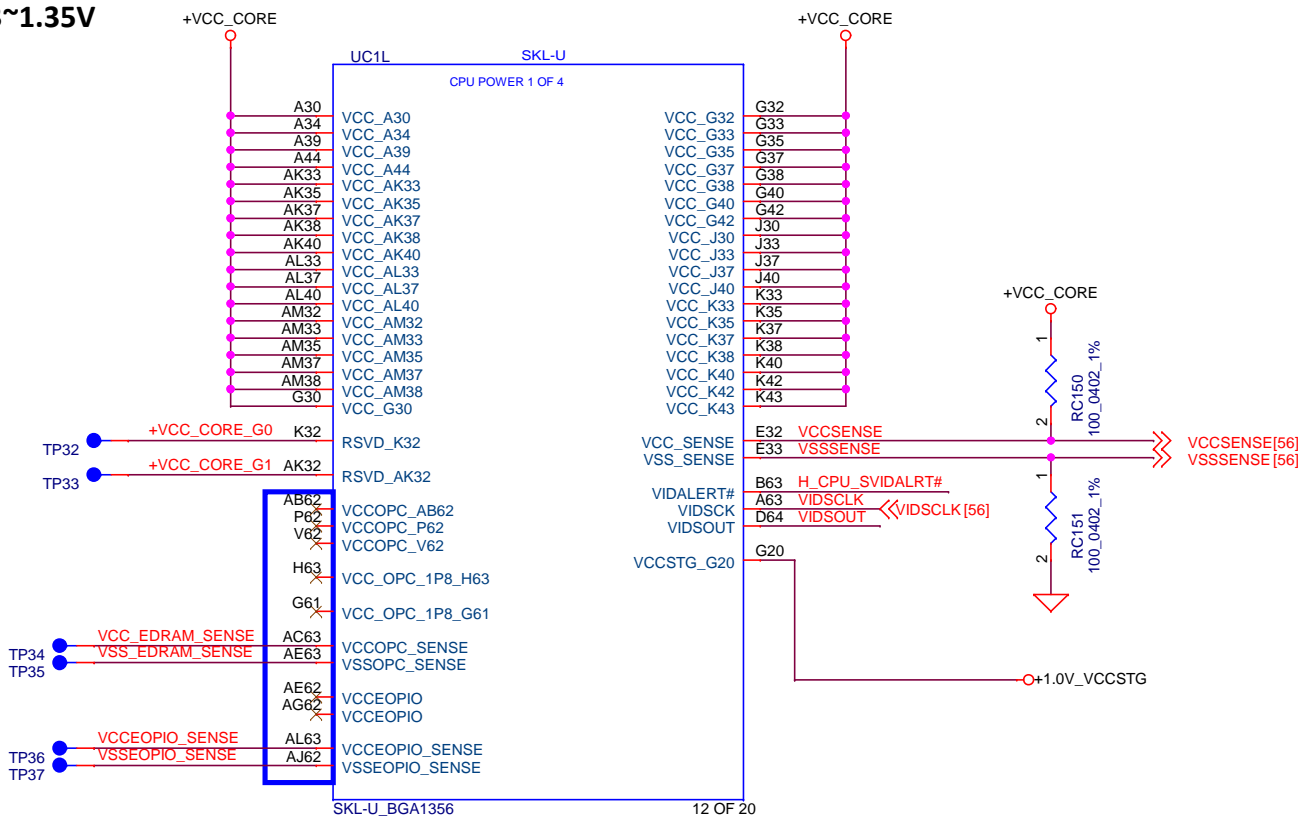
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Title		MCP(9/14)XDP	
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+VCC_CORE: 0.3~1.35V

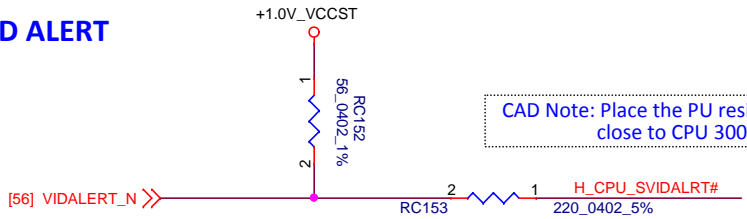


VCCOPC,VCCOPC_1P8,VCCEPIO for SKYLake-U 2+3e
(w/ on package cache)

PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

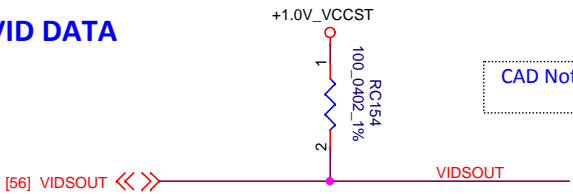
Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

SVID ALERT



CAD Note: Place the PU resistors close to CPU
close to CPU 300 - 1500mils

SVID DATA



CAD Note: Place the PU resistors close to CPU
close to CPU 300 - 1500mils

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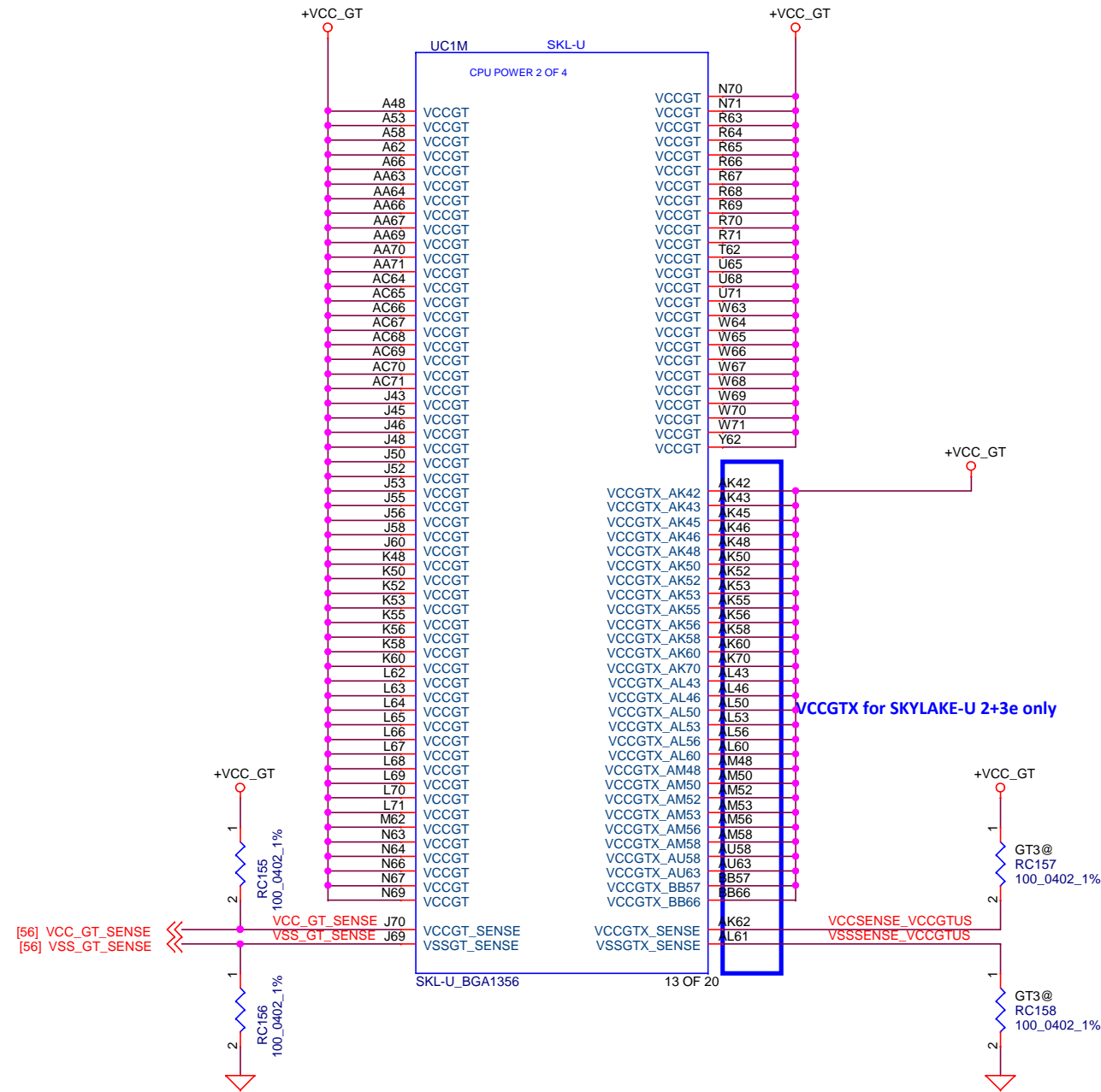
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Title			MCP(10/14)PWR-VCC CORE	
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+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V



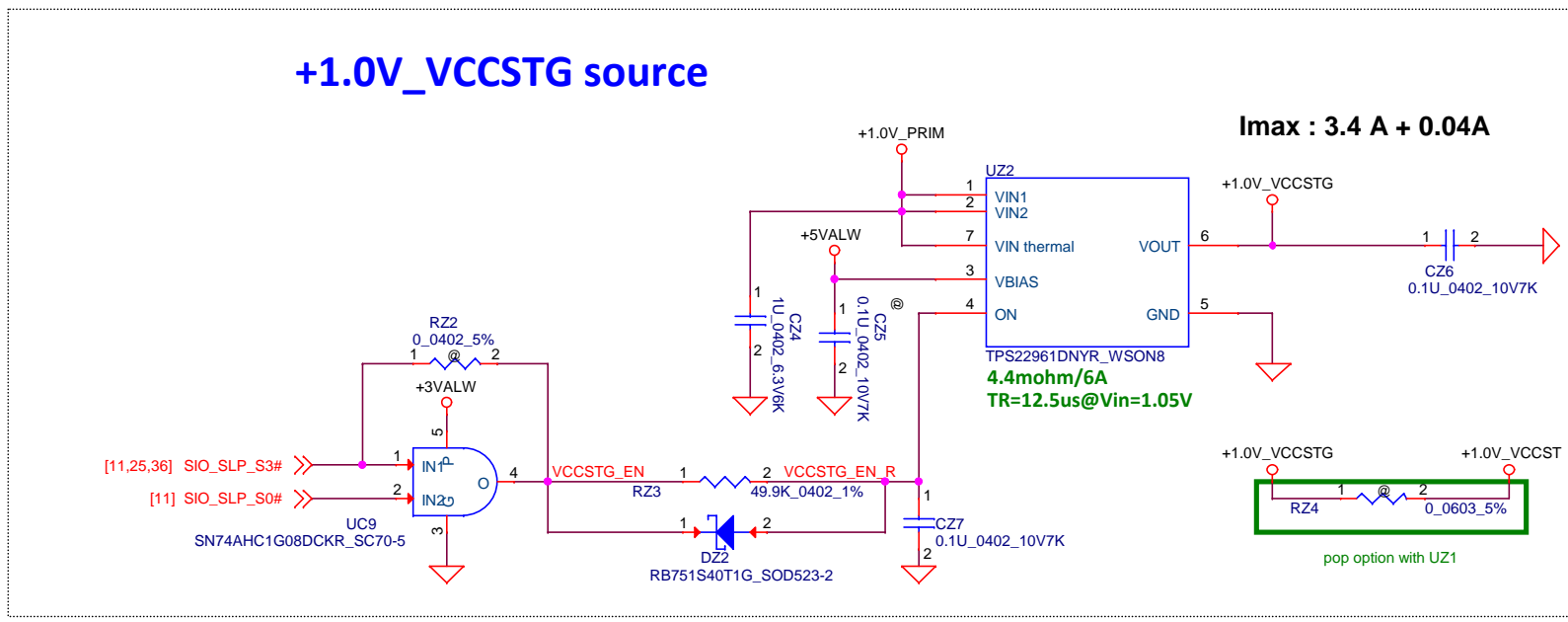
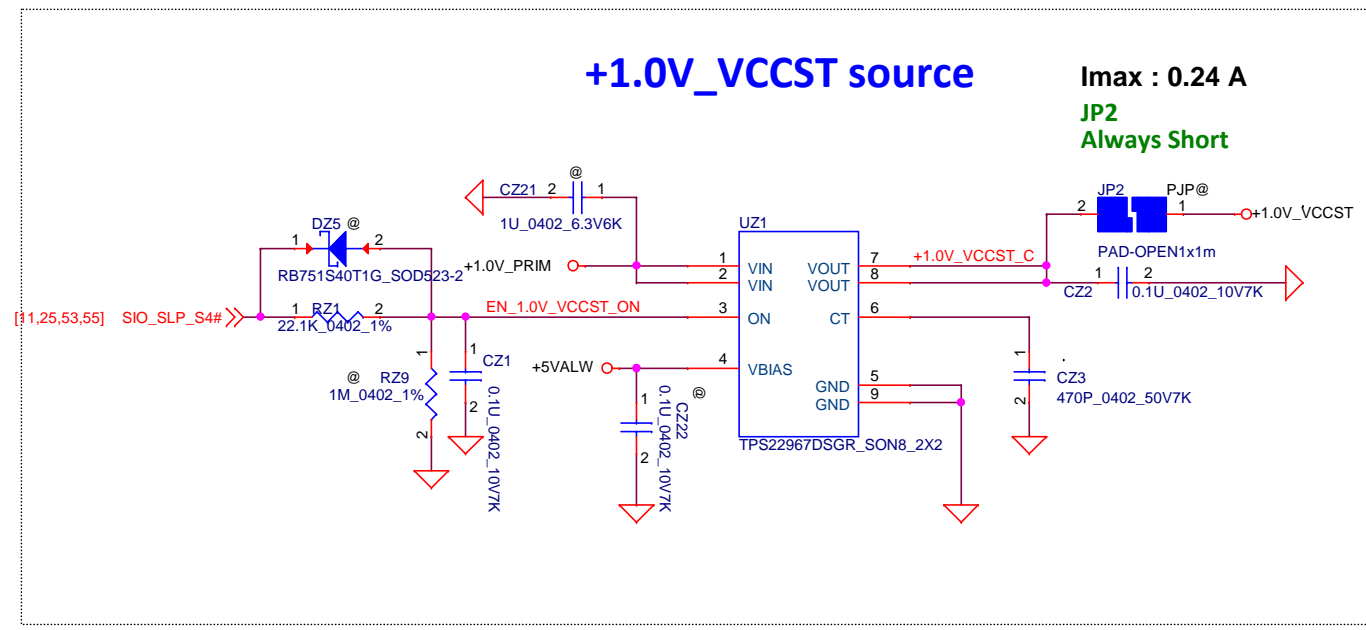
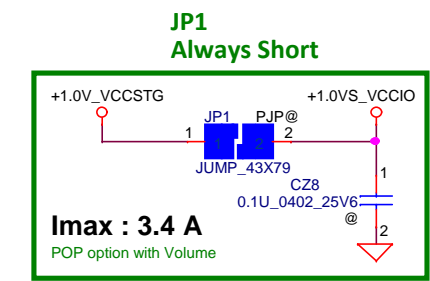
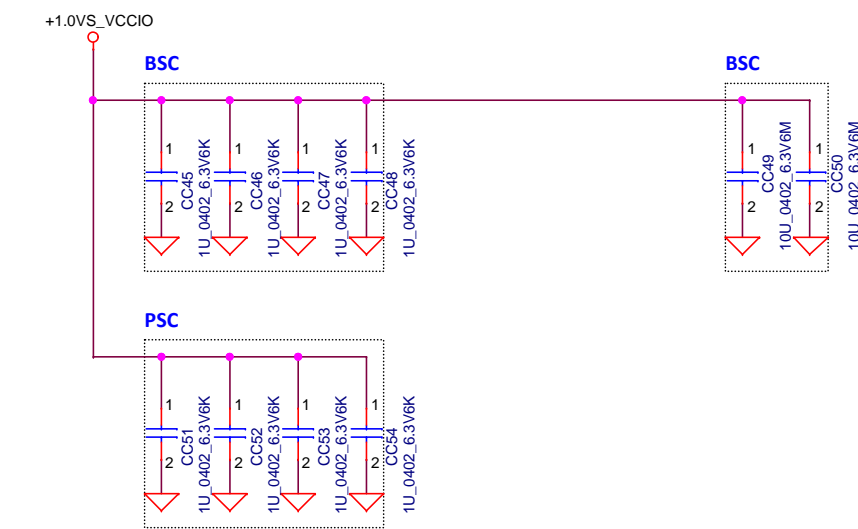
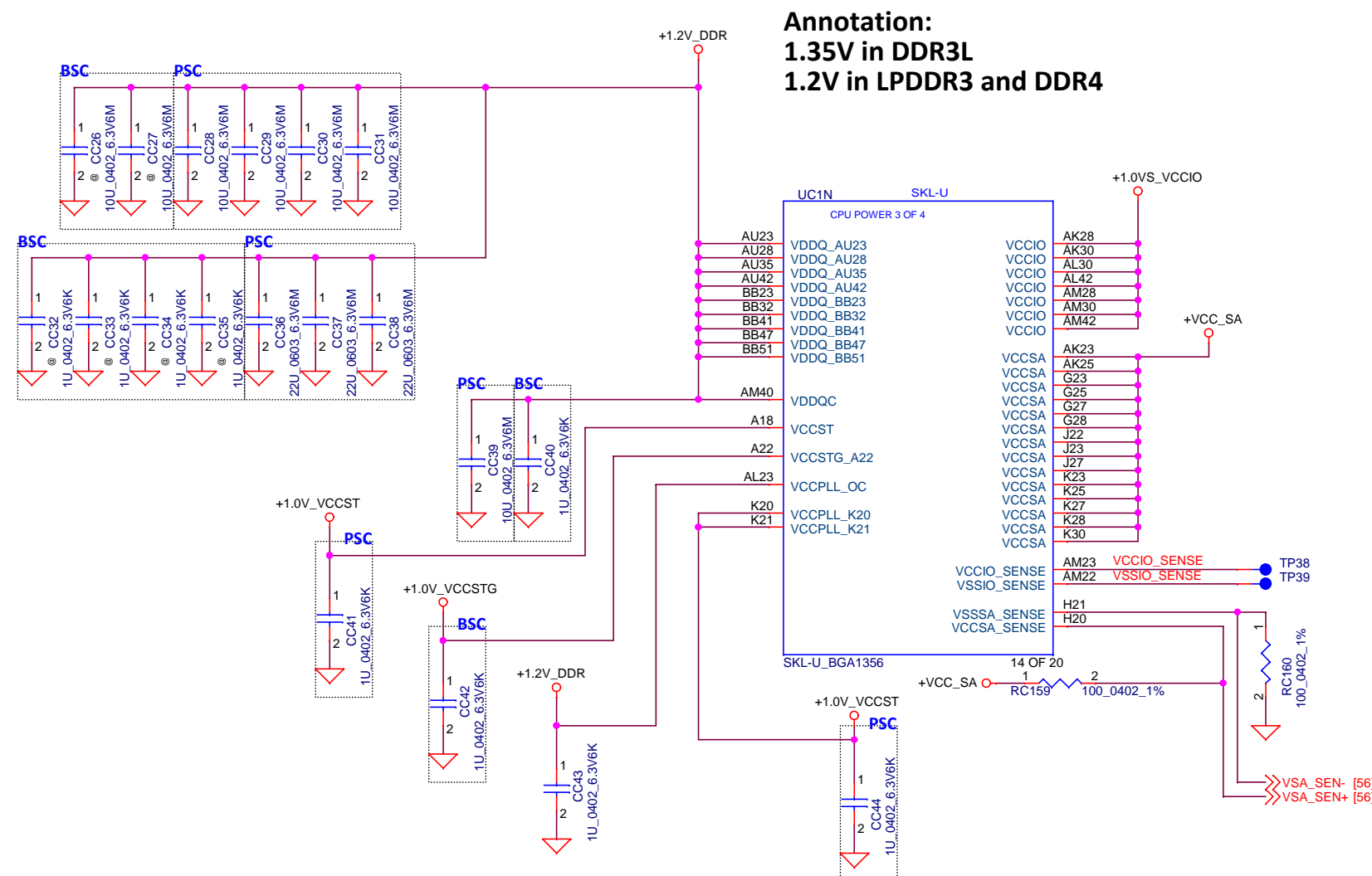
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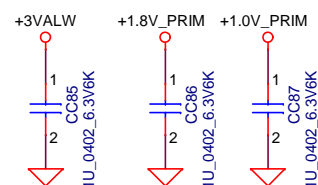
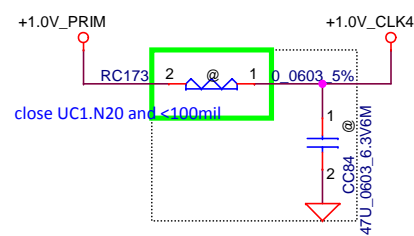
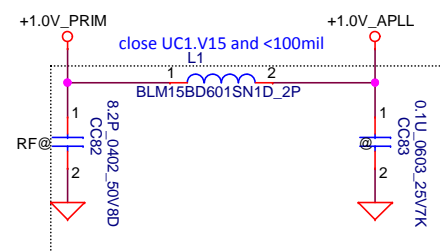
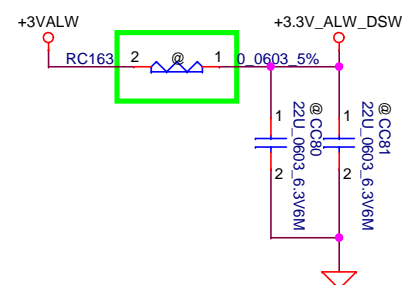
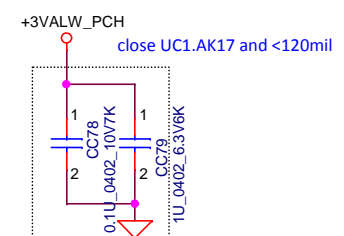
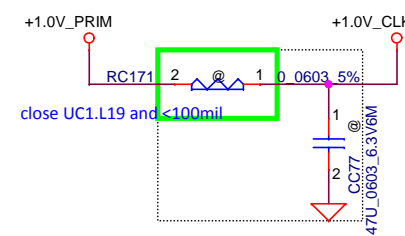
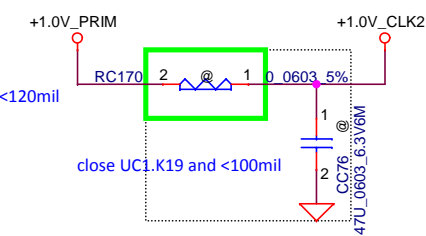
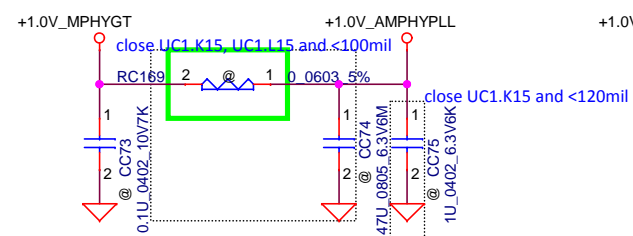
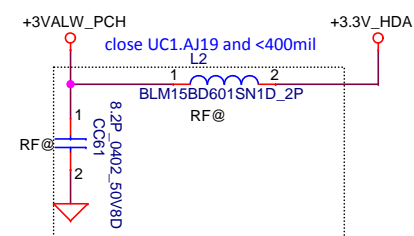
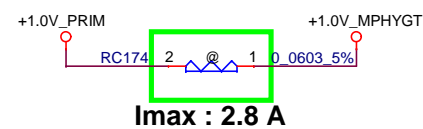
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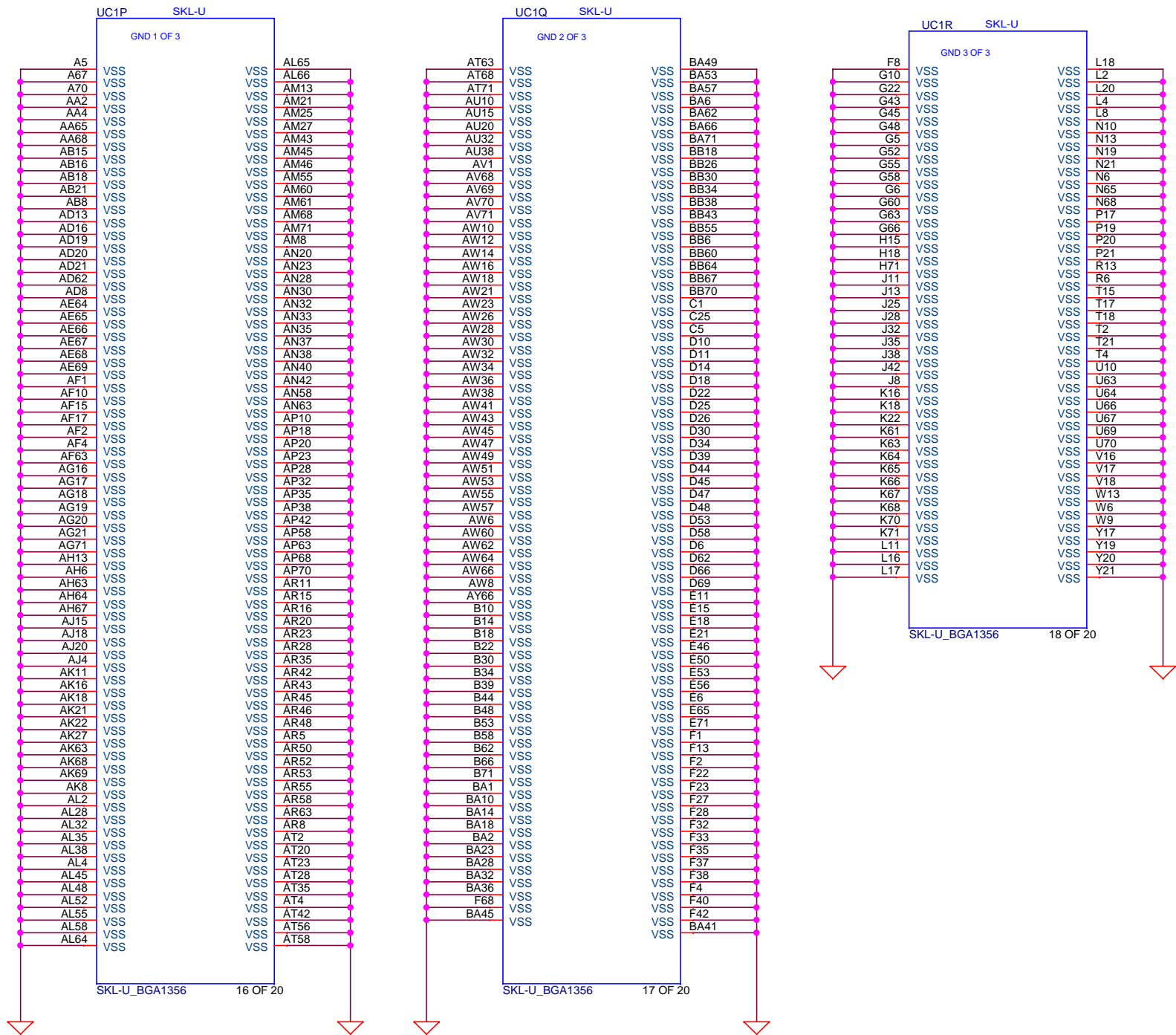
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Title			
MCP(13/14)PCH PWR			
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For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

DELL CONFIDENTIAL/PROPRIETARY

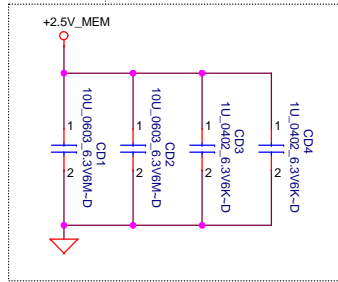
Compal Electronics, Inc.



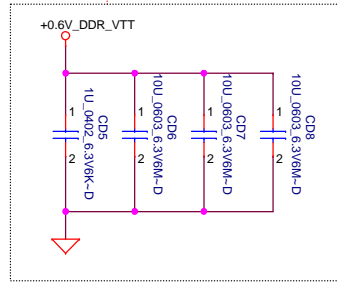
Title		
MCP(14/14)VSS		
Size	Document Number	Rev
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Layout Note:
Place near JDIMM1.257,259

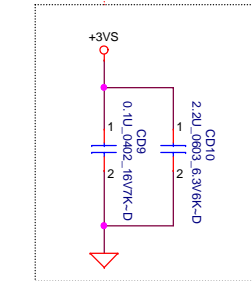


Layout Note:
Place near JDIMM1.258

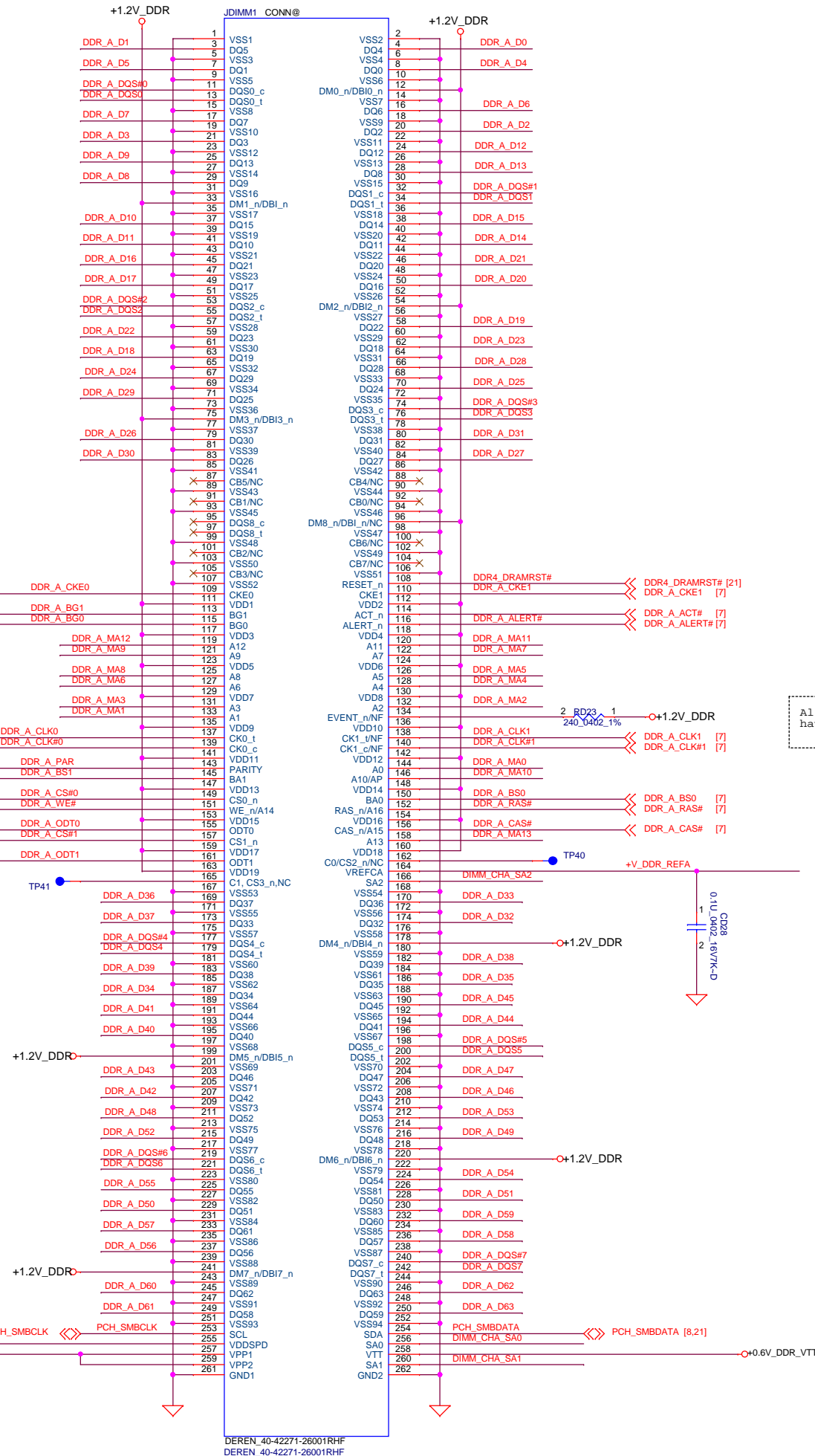
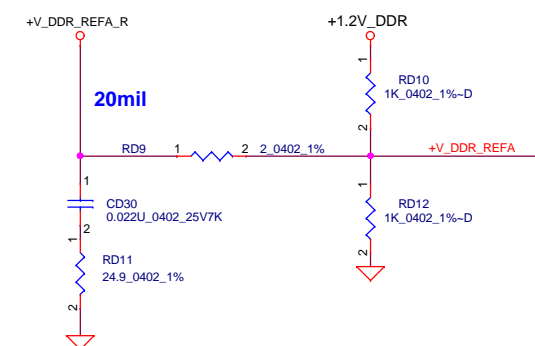
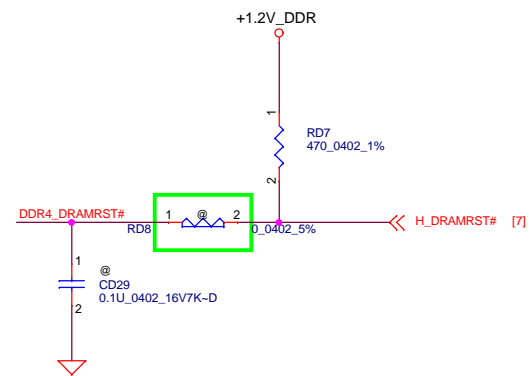
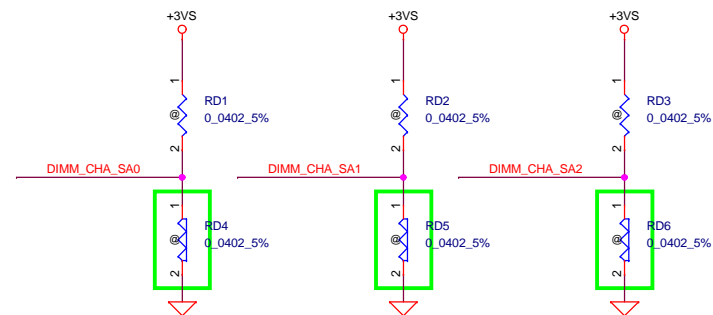
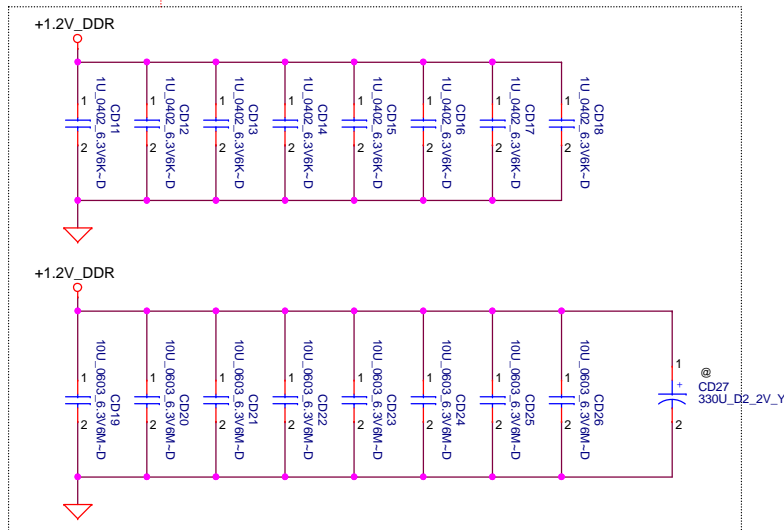


[7] DDR_A_D[0..63]
[7] DDR_A_MA[0..13]
[7] DDR_A_DQS#[0..7]
[7] DDR_A_DQS[0..7]

Layout Note:
Place near JDIMM1.255



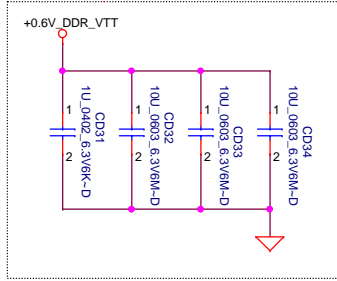
Layout Note:
Place near JDIMM1



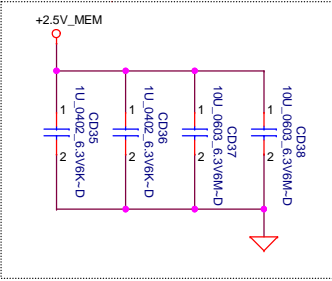
All VREF traces should
have 10 mil trace width

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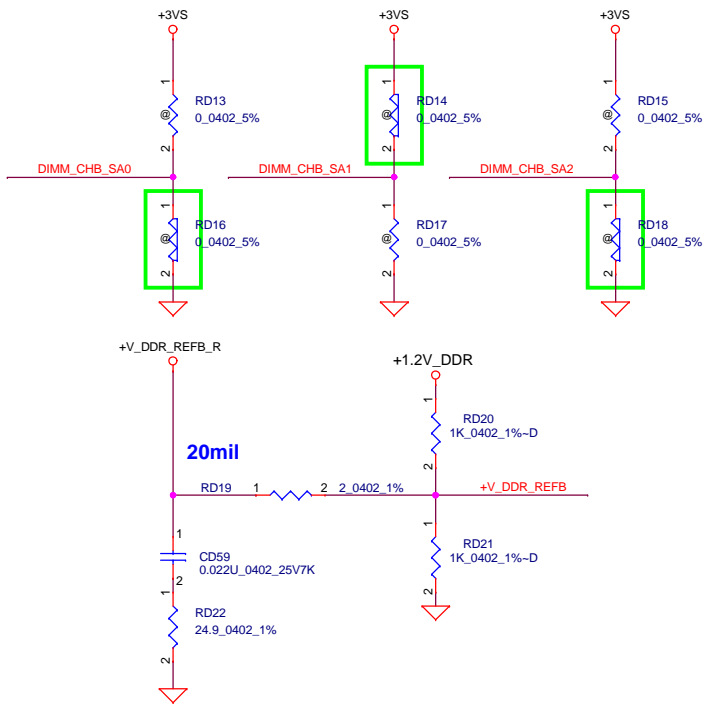
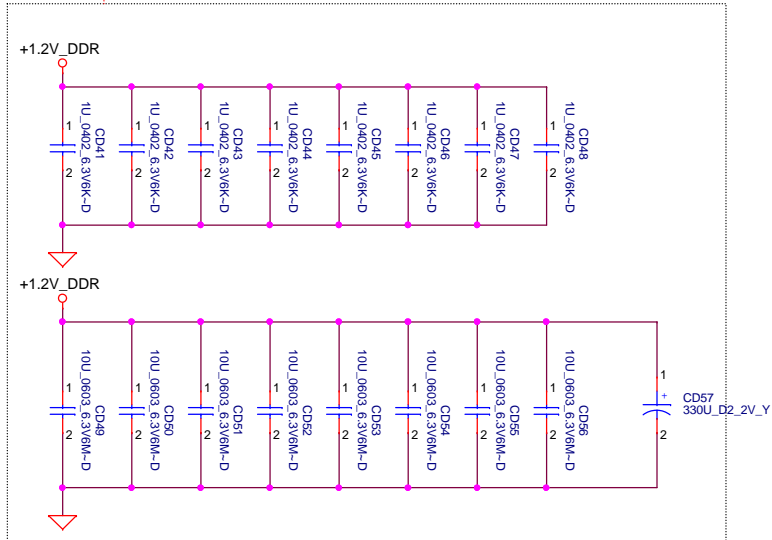
Layout Note:
Place near JDIMM2.258



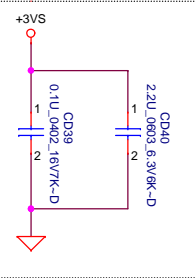
Layout Note:
Place near JDIMM2.257,259



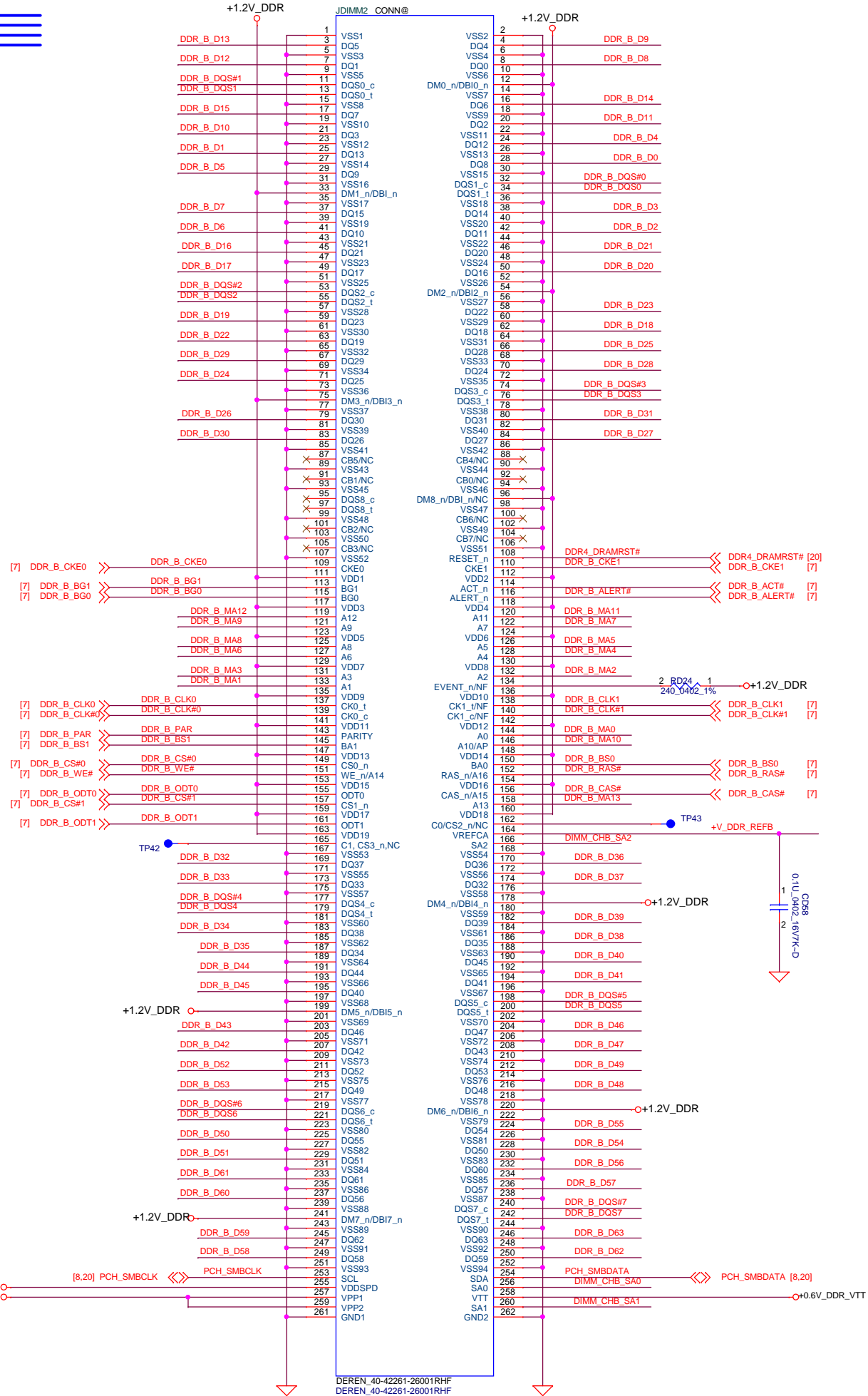
Layout Note:
Place near JDIMM2



```
[7] DDR_B_D[0..63]
[7] DDR_B_MA[0..13]
[7] DDR_B_DQS#[0..7]
[7] DDR_B_DQS[0..7]
```



Layout Note:
Place near JDIMM2.255



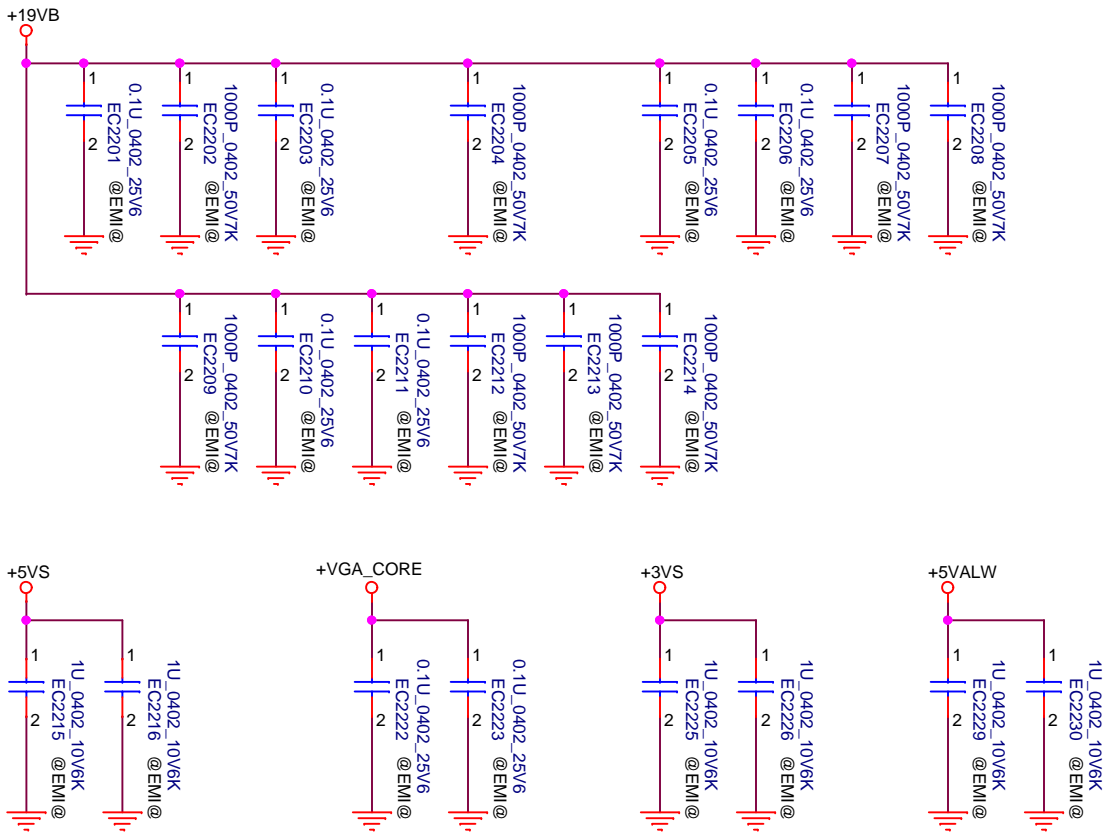
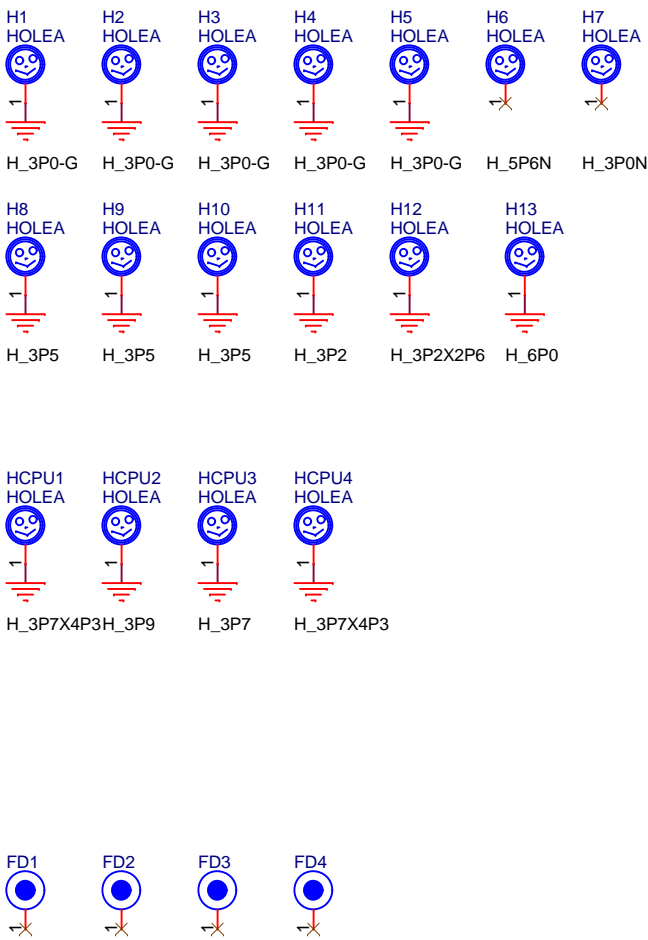
All VREF traces should
have 10 mil trace width

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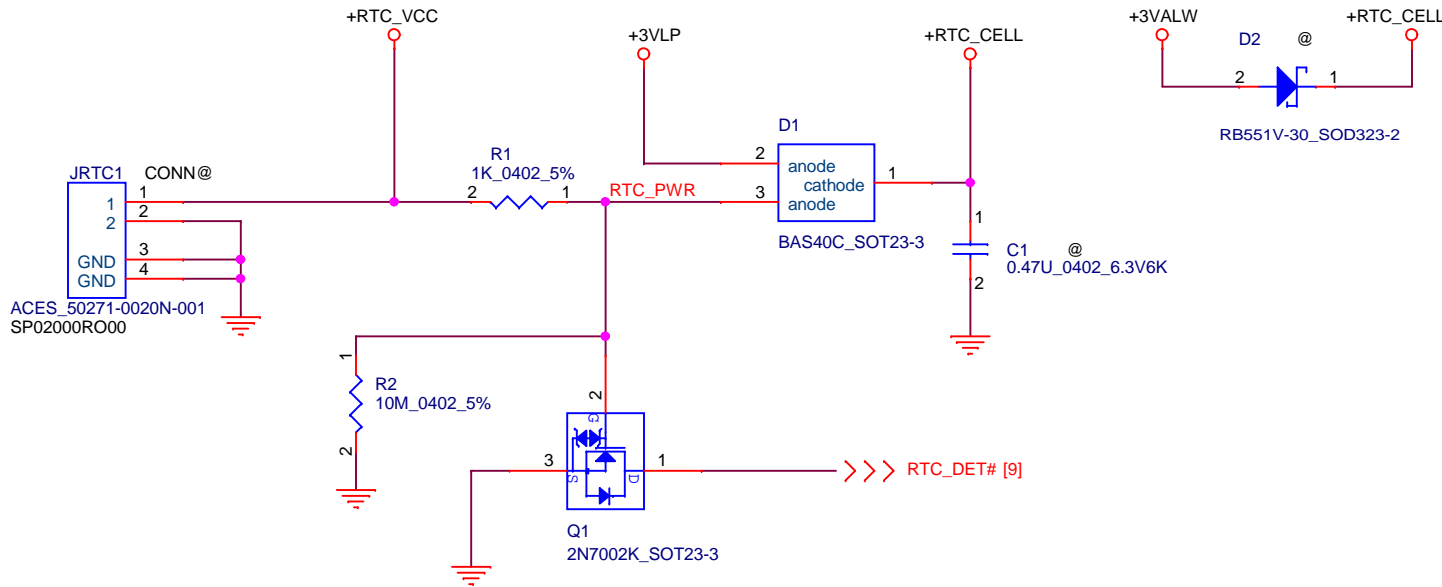
Main Func = Other

Mind the voltage rating of the caps.

Screw hole/FD

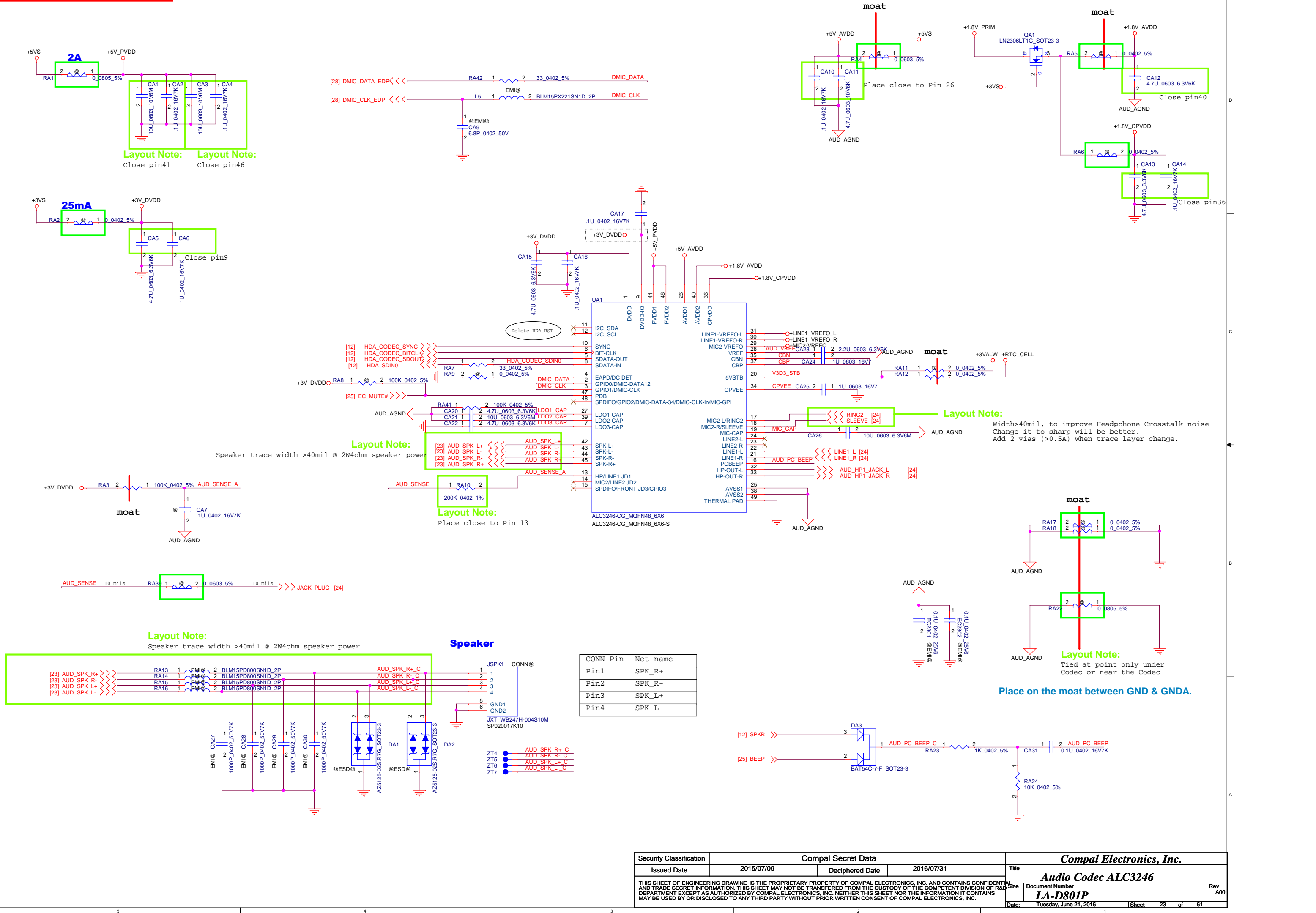


Main Func = RTC

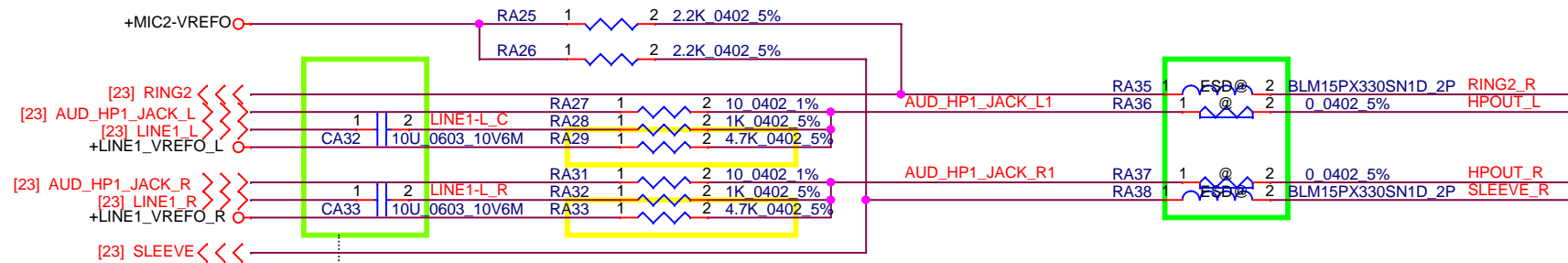


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Main Func = Audio



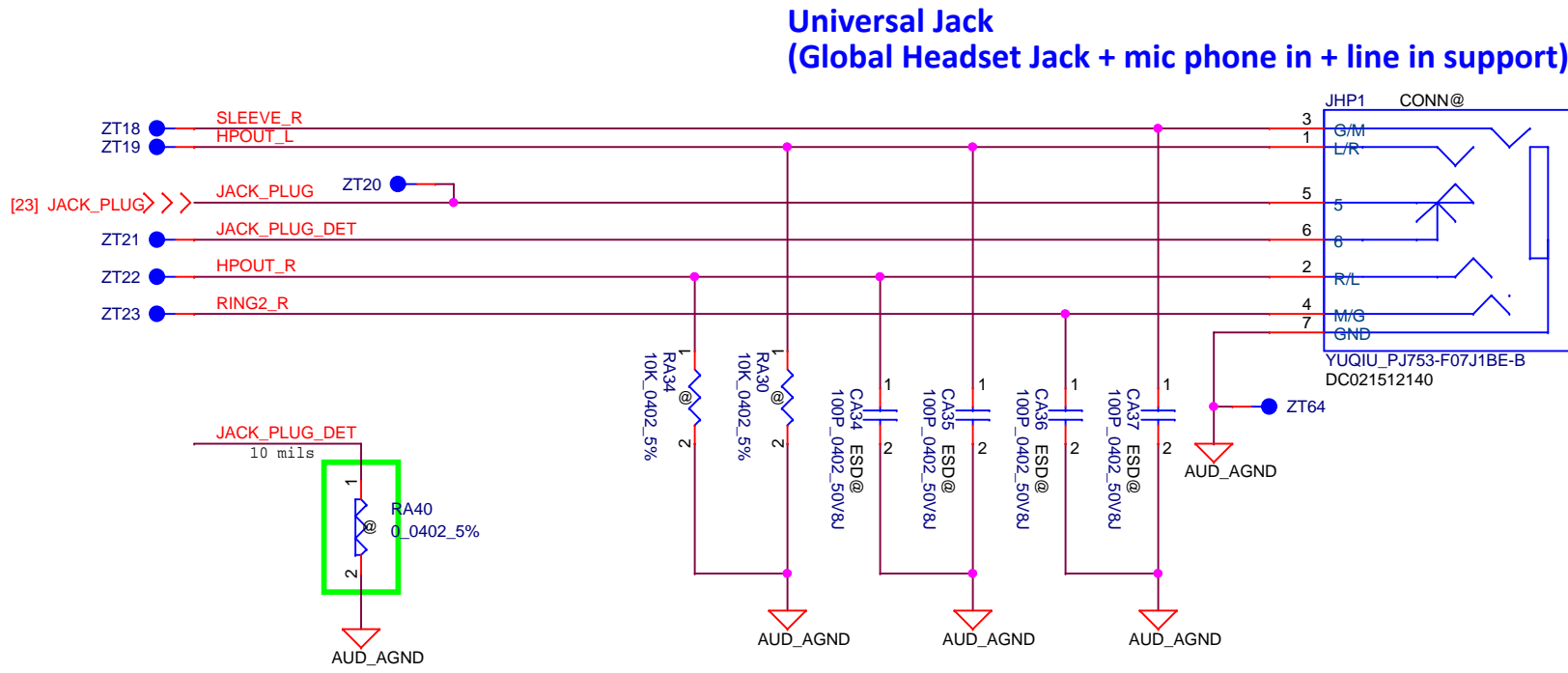
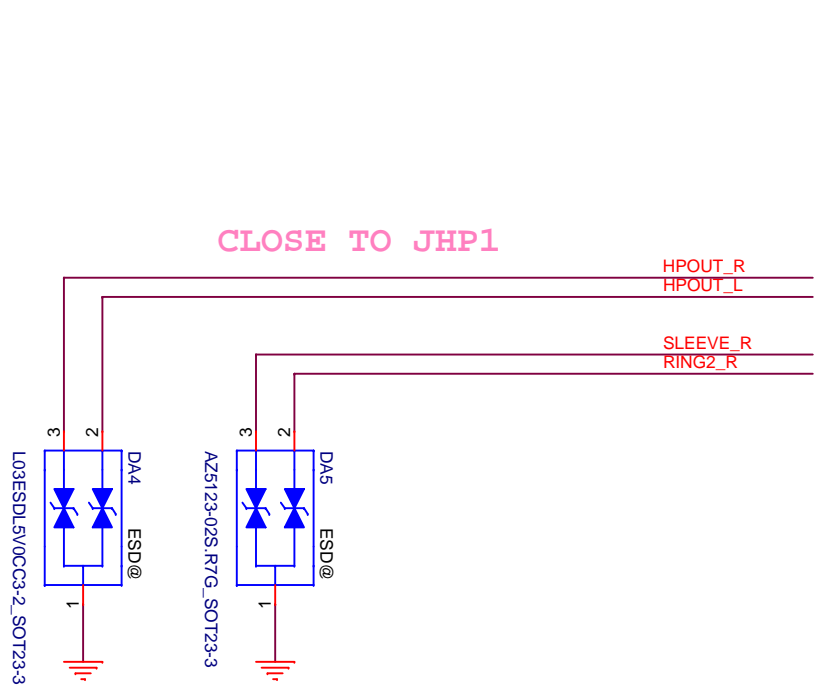
Main Func = Audio Jack



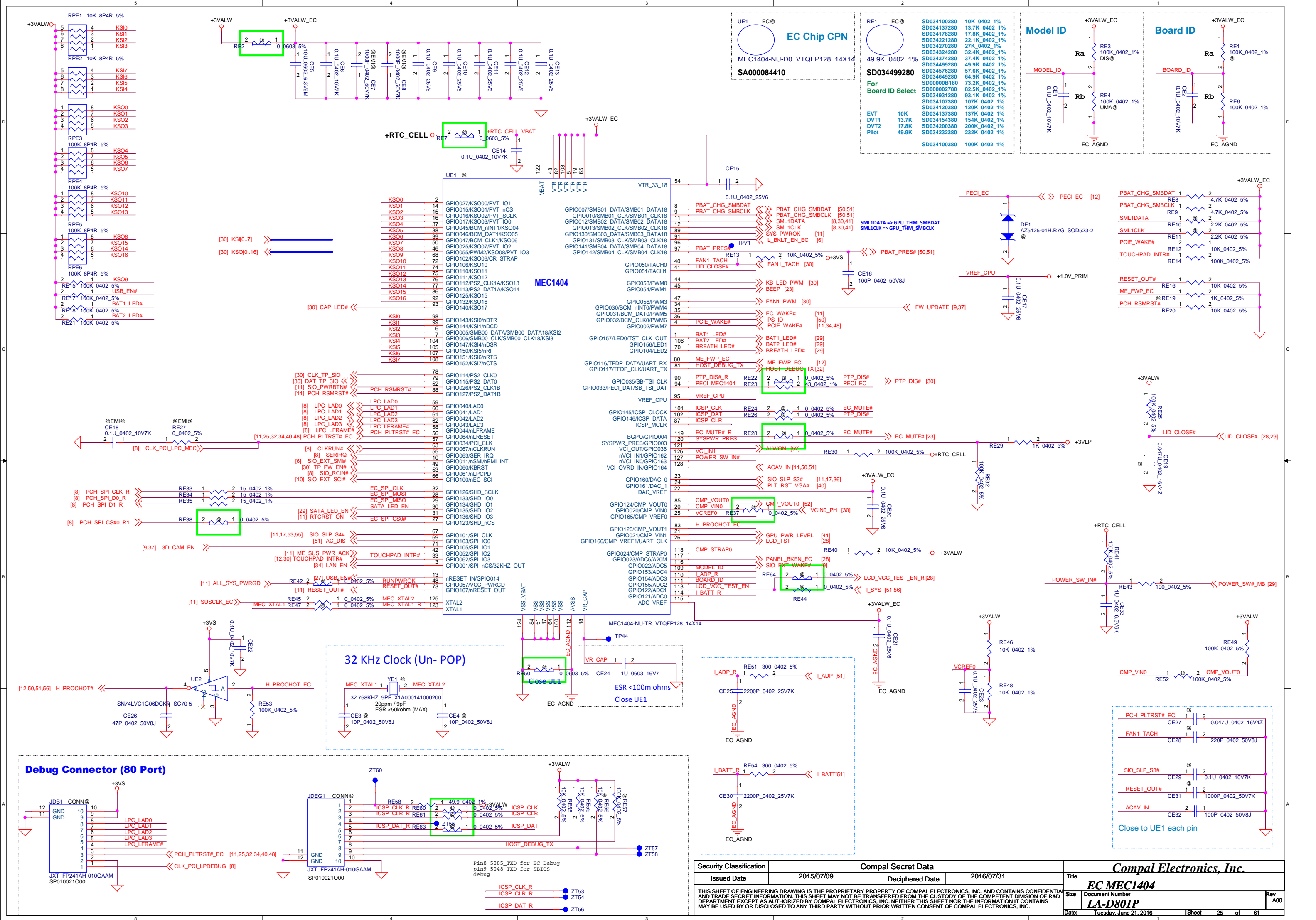
Layout Note:
Close to UA1

Universal Jack
(Global Headset Jack + mic phone in + line in support)

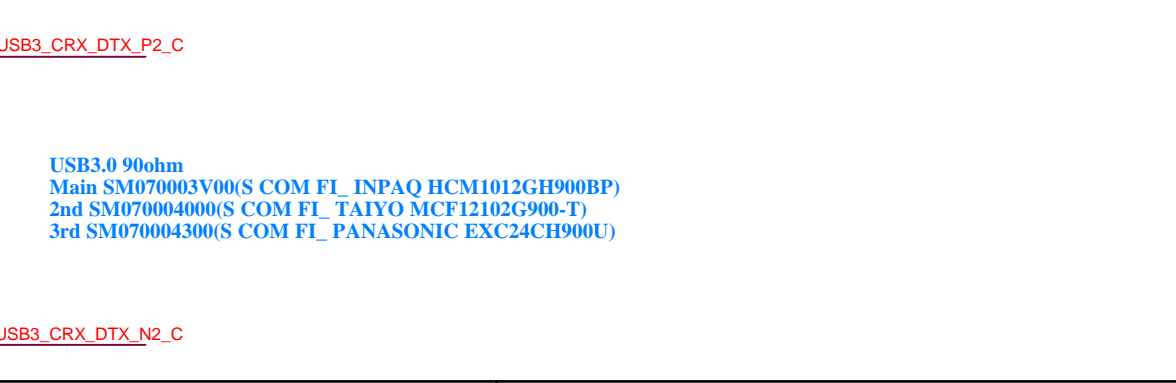
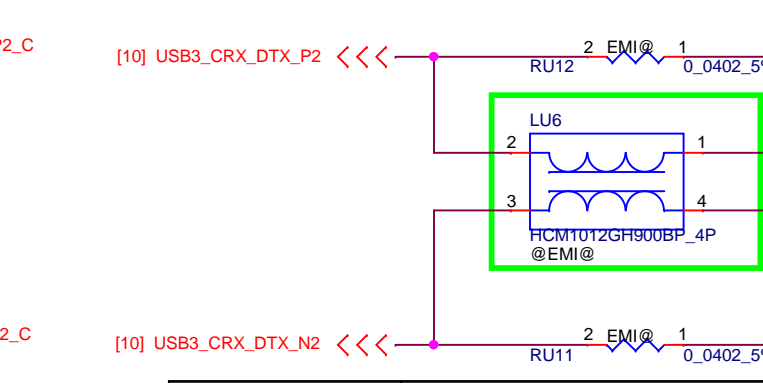
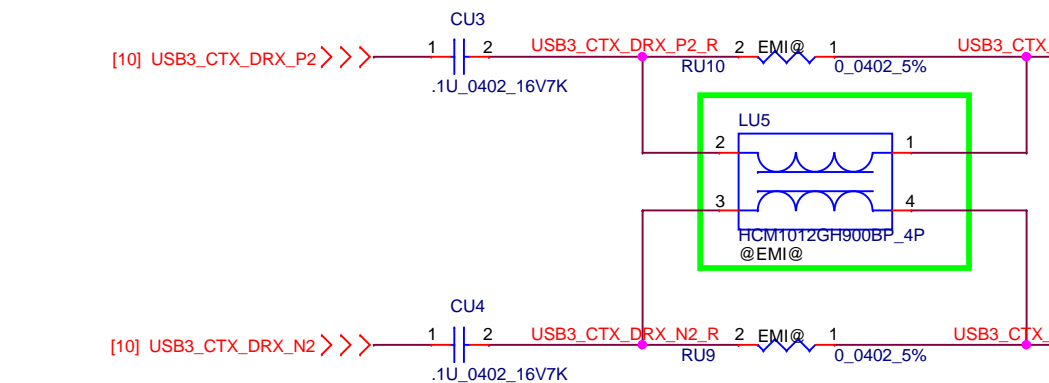
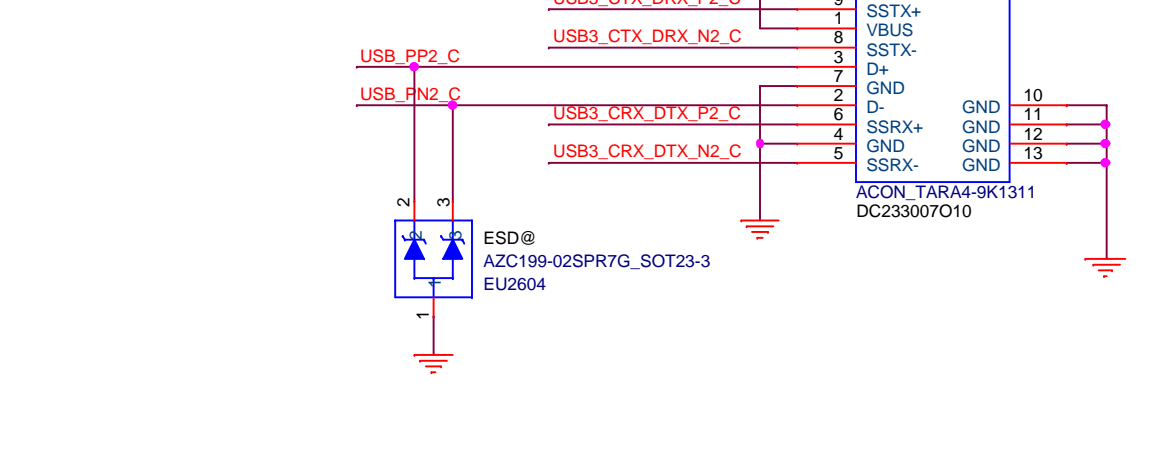
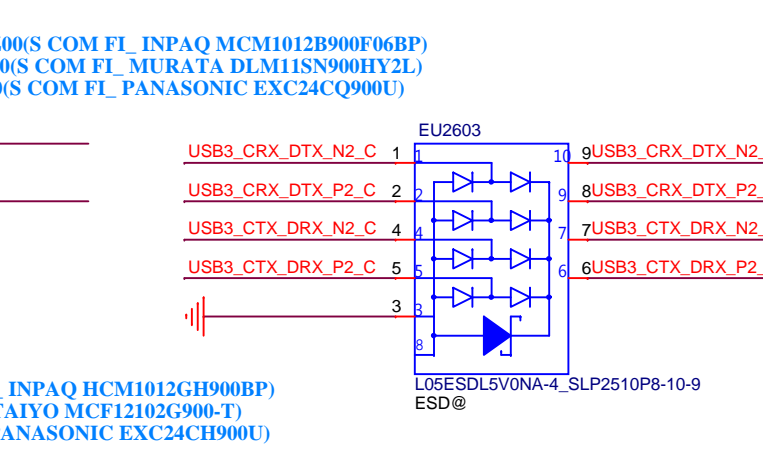
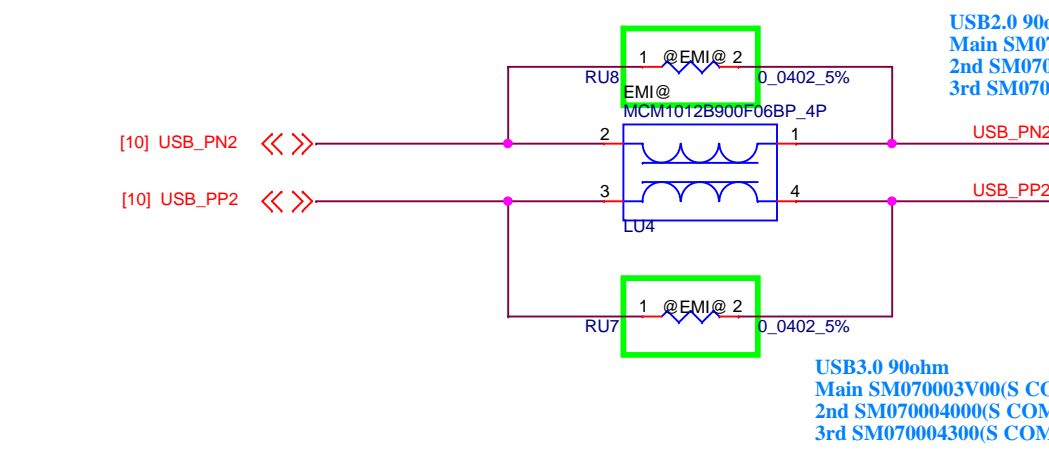
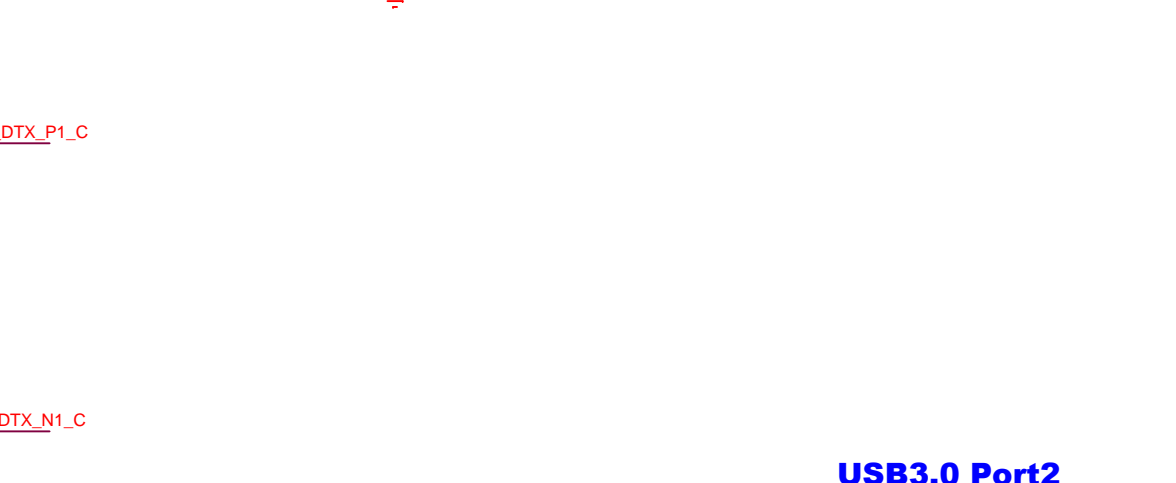
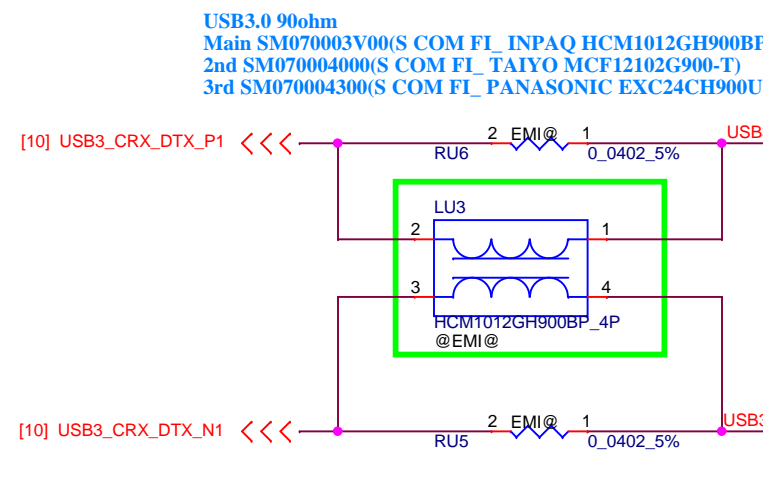
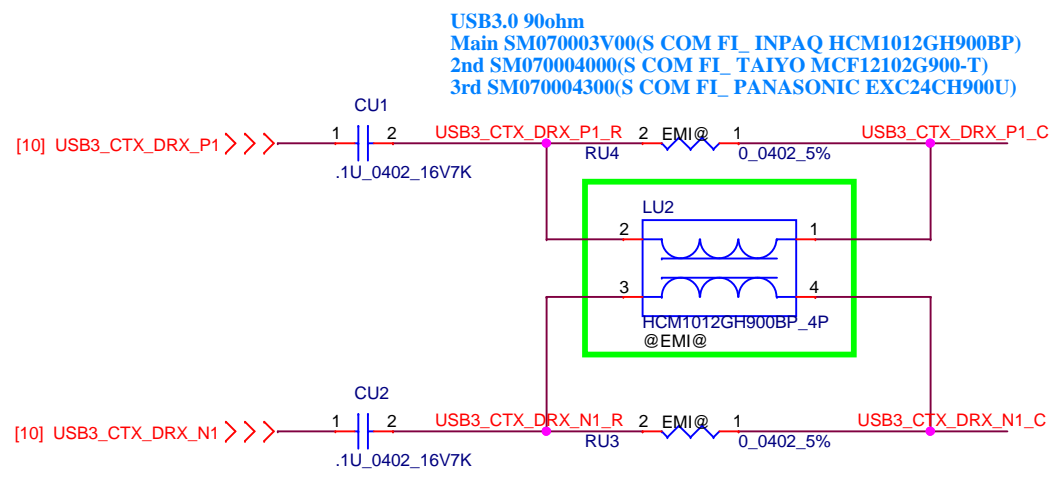
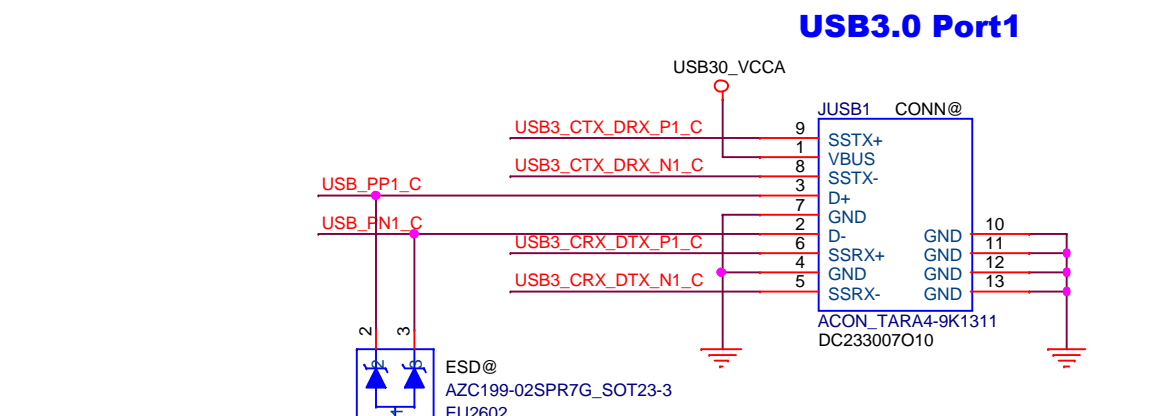
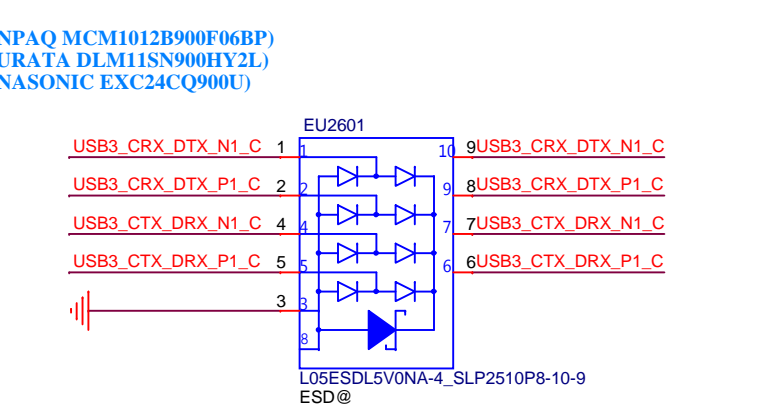
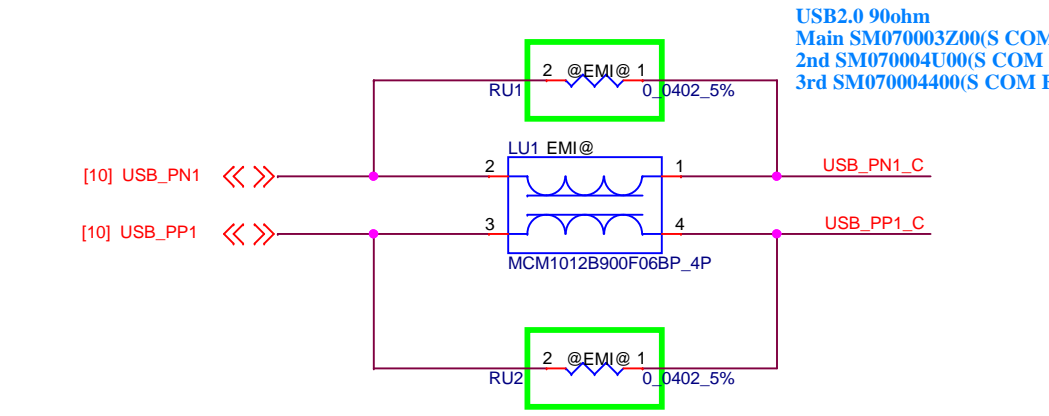
Main Func = Audio Jack



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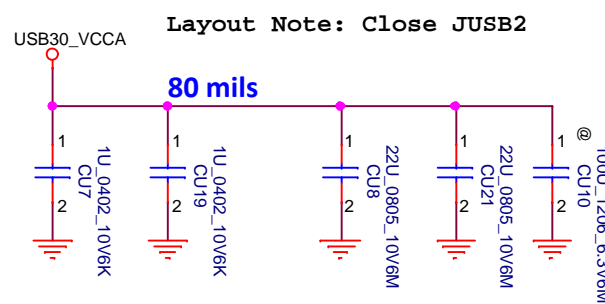
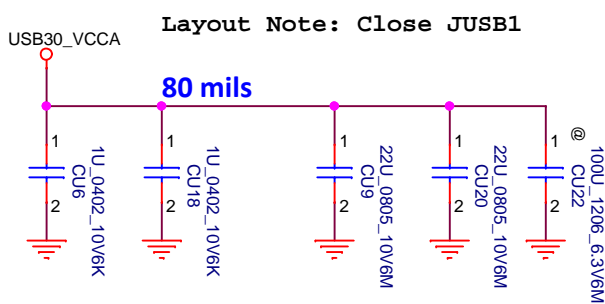
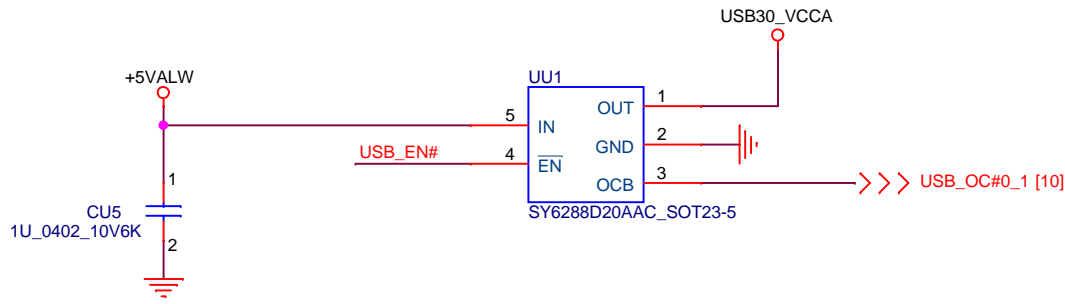
Main Func = USB3.0 Port1



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				Date:	Tuesday, June 21, 2016	Sheet 26 of 61

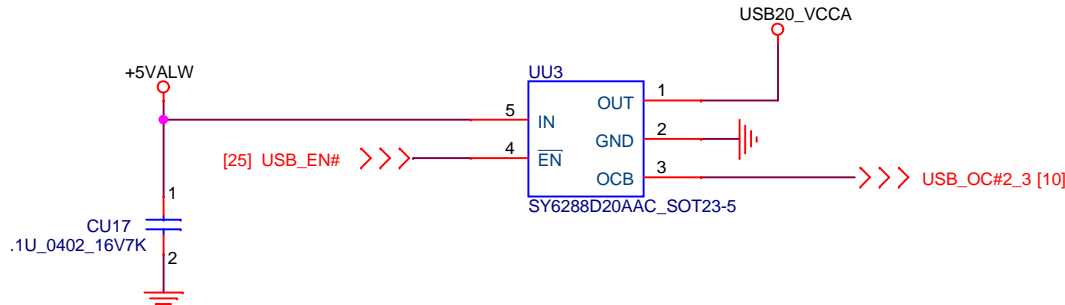
Main Func = USB3.0 Port1/Port2

SY6288D Support 2A

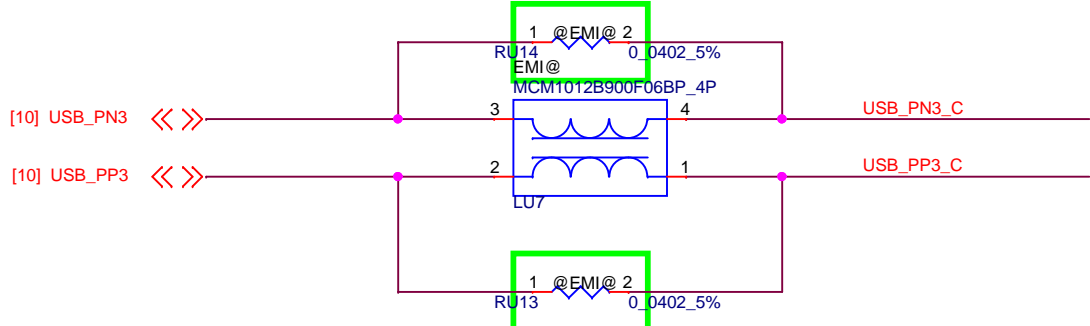


Main Func = USB3.0 Port3

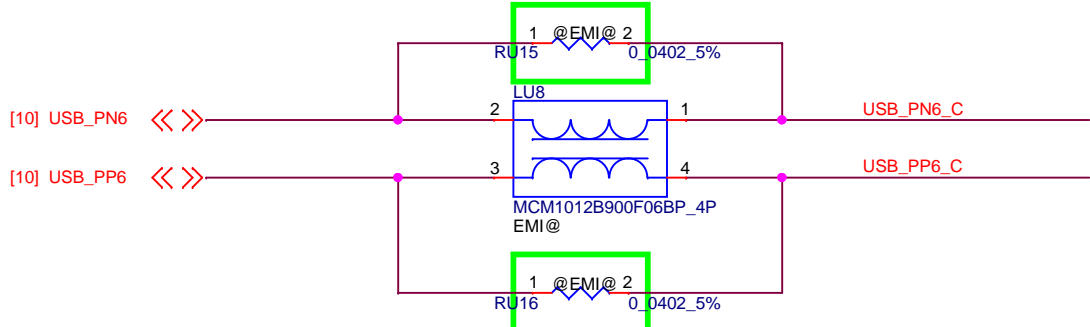
SY6288D Support 2A



USB2.0

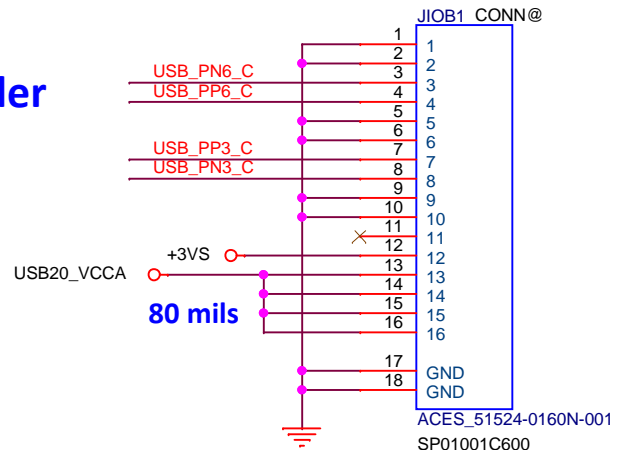


CardReader

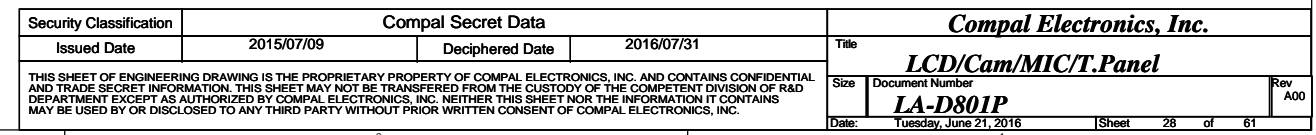
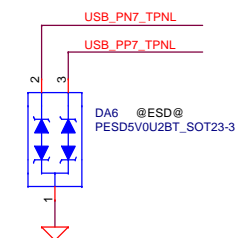


I/O Board Connector

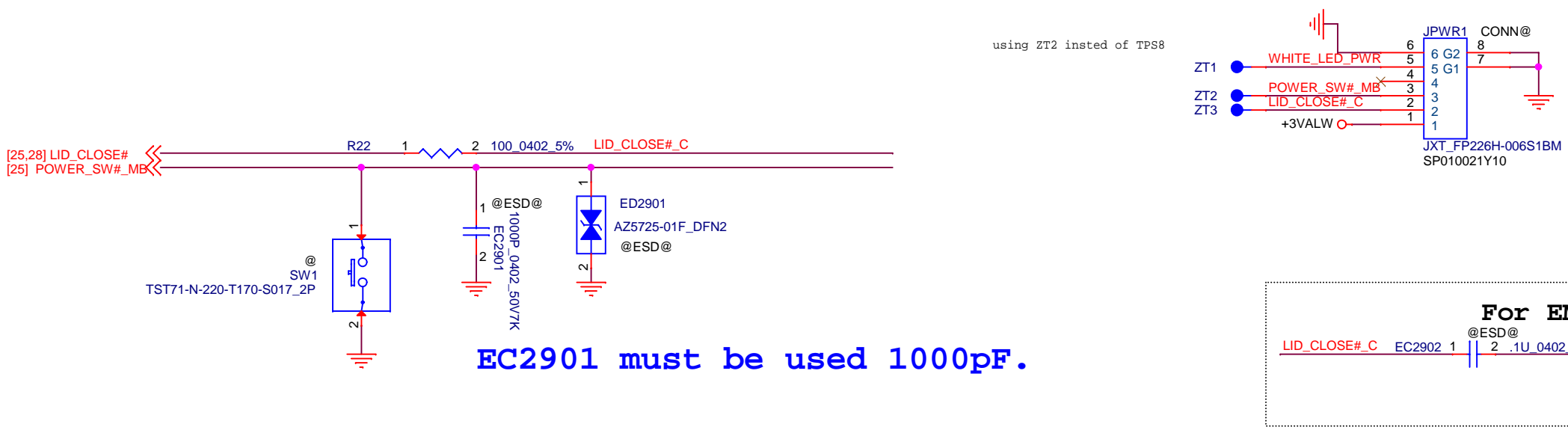
CardReader
USB2.0



INVERTER POWER



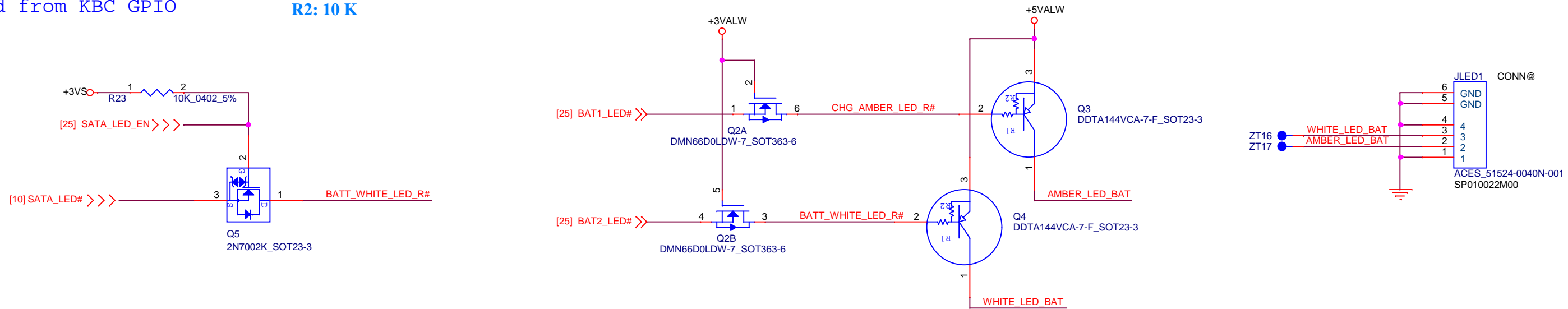
Main Func = Power BTN



Main Func = Battery LED

Low actived from KBC GPIO

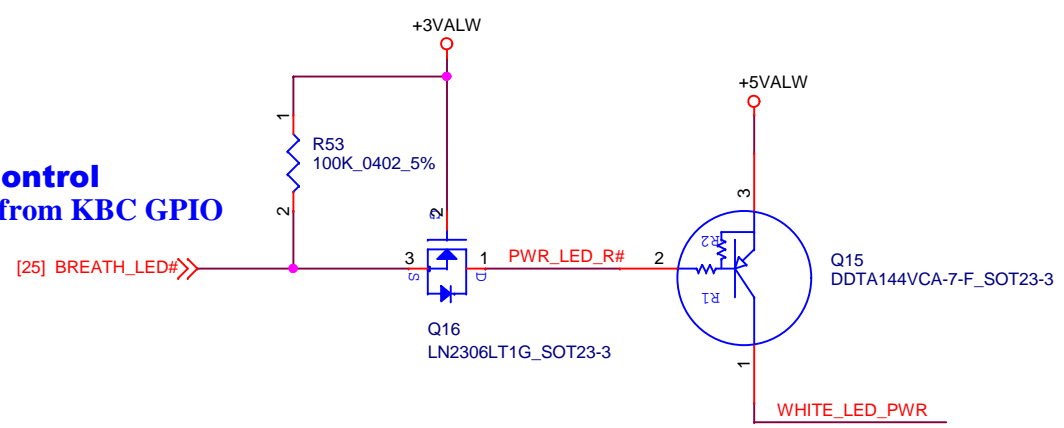
BJT
R1: 47 K
R2: 10 K



Main Func = PWR LED

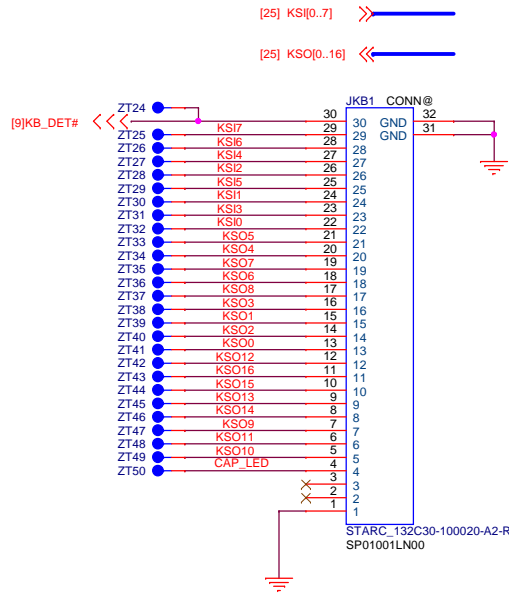
Low actived from KBC GPIO

PWR LED Control
LOW actived from KBC GPIO

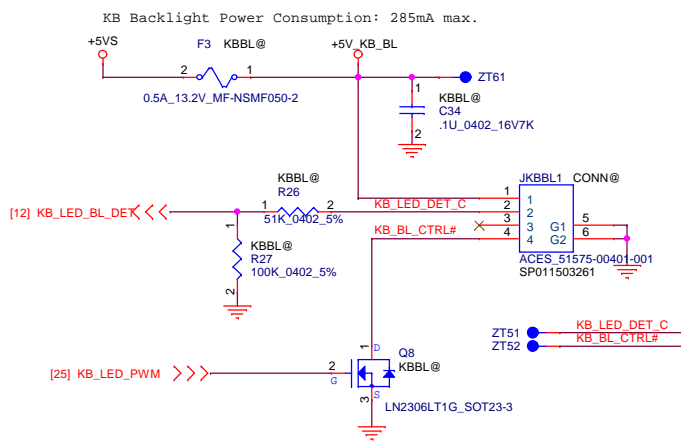


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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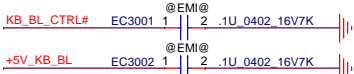
Main Func = KB



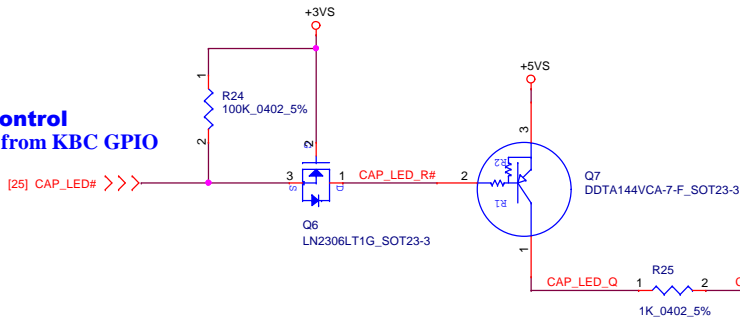
Keyboard Backlight (Reserved)



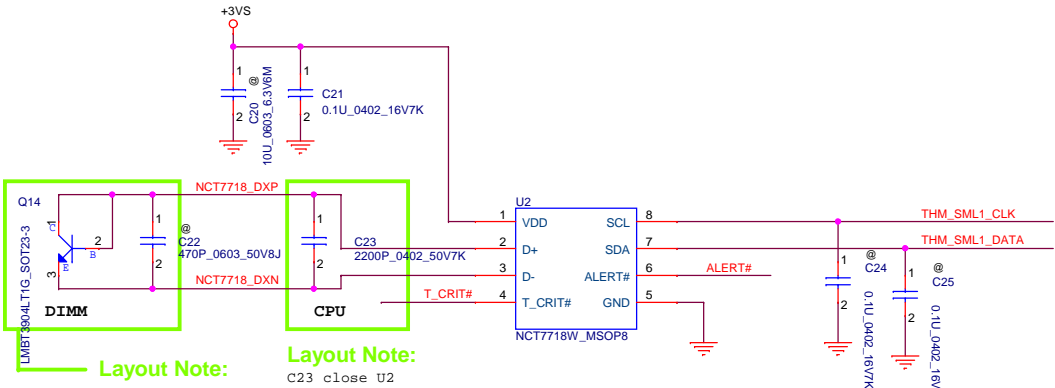
For EMI Reserved



CAP LED Control
LOW acted from KBC GPIO



Main Func = Thermal

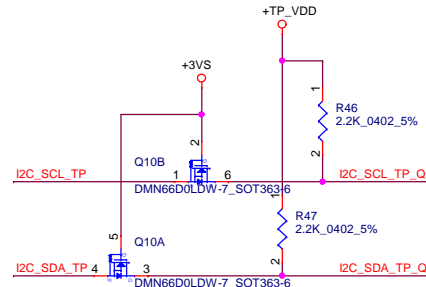
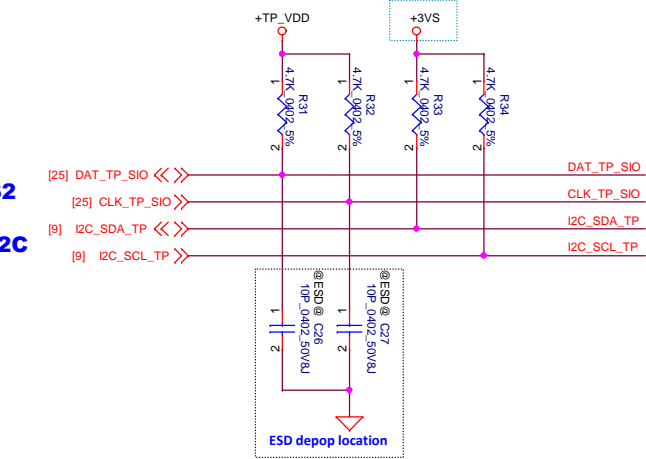


DXN and DXP routing width and spacing is 10 mil / 10 mil.

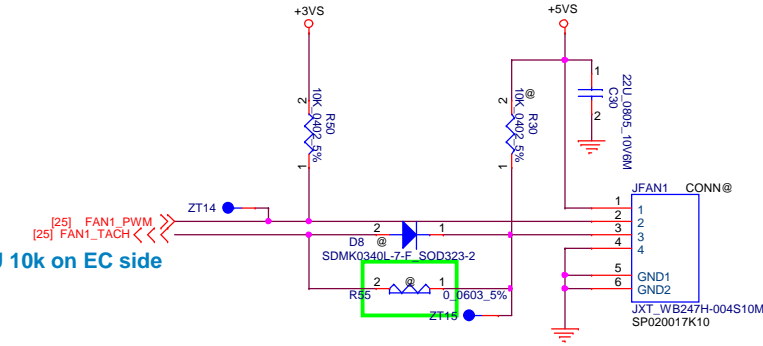
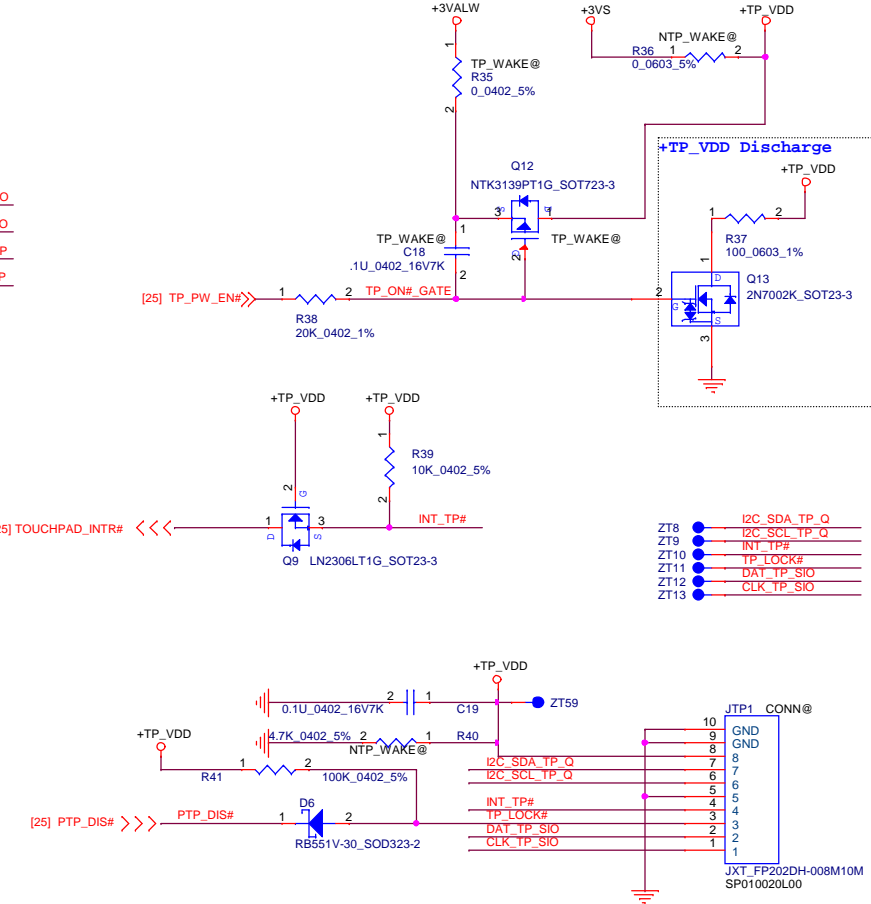
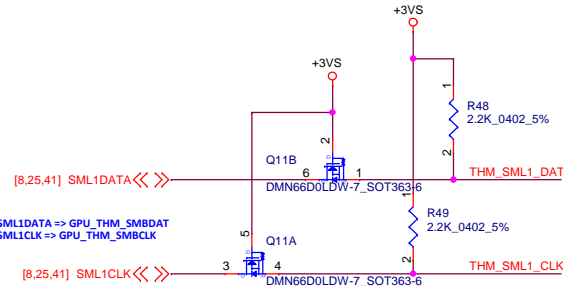
TEMPERATURE (°C)	T_CRIT#					
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ	
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Main Func = TPAD

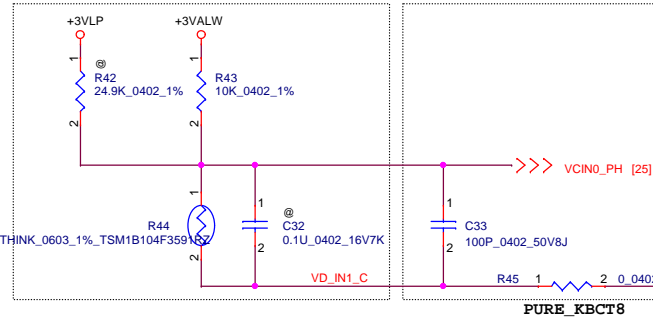
EC/PS2
PCH/I2C



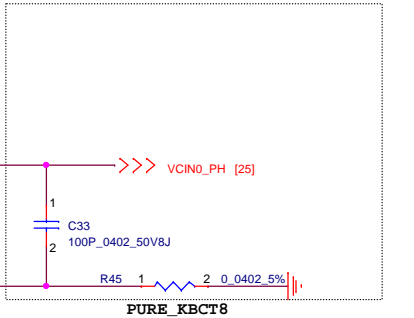
"FAN1_FB" PU 10k on EC side



Close to Thermal sensor

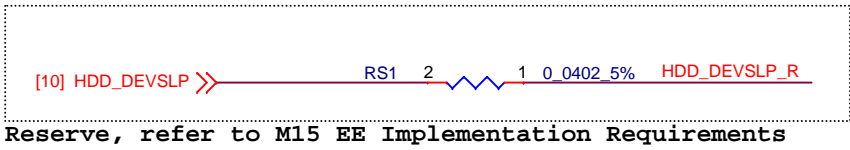
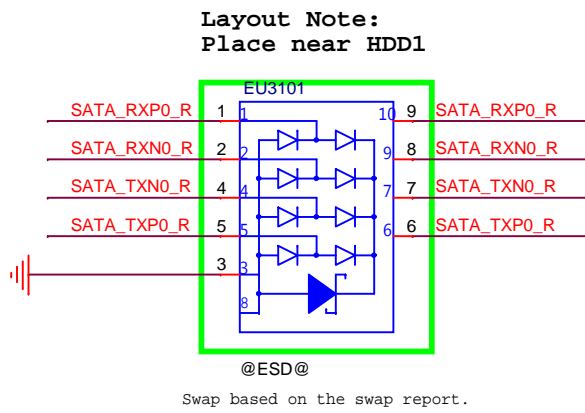


Close to KBC
VD_IN1 for system thermal sensor

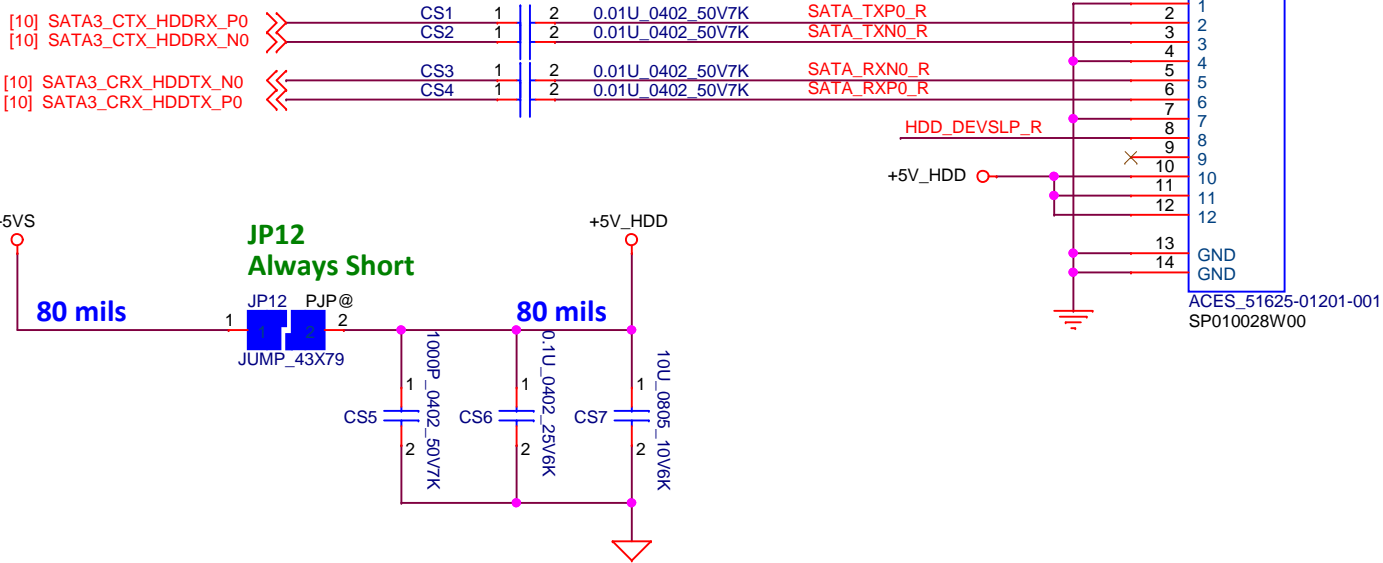


Main Func = HDD

SATA HDD Connector



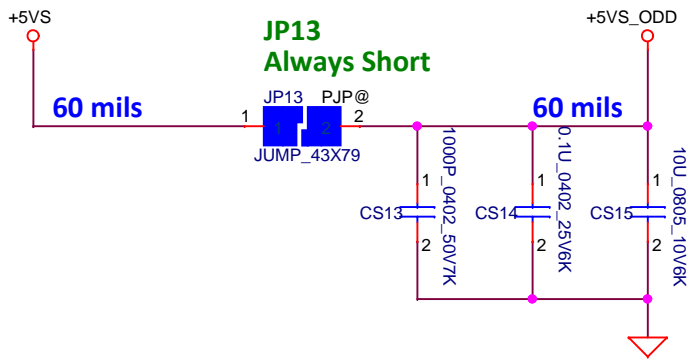
SOC TX
SOC RX



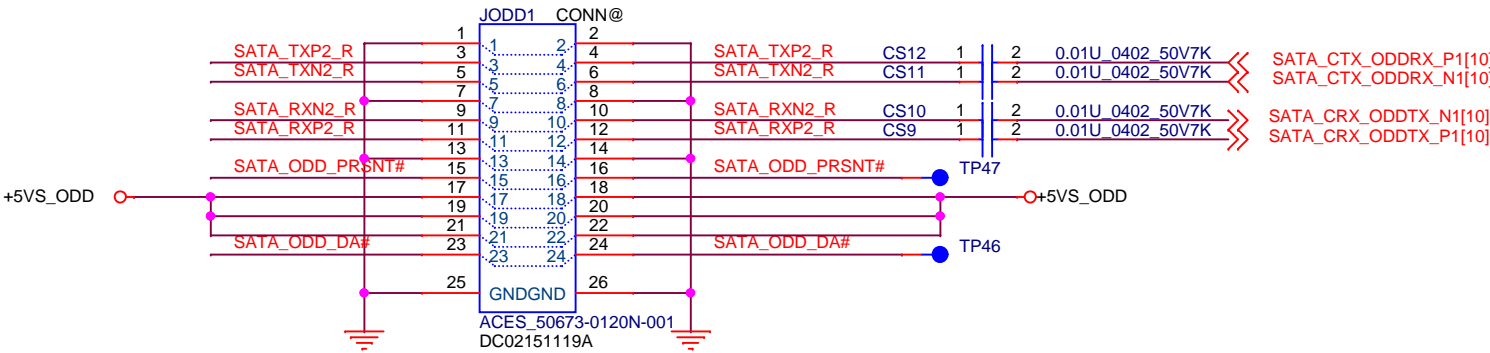
CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

Main Func = ODD

ODD ZiF Connector

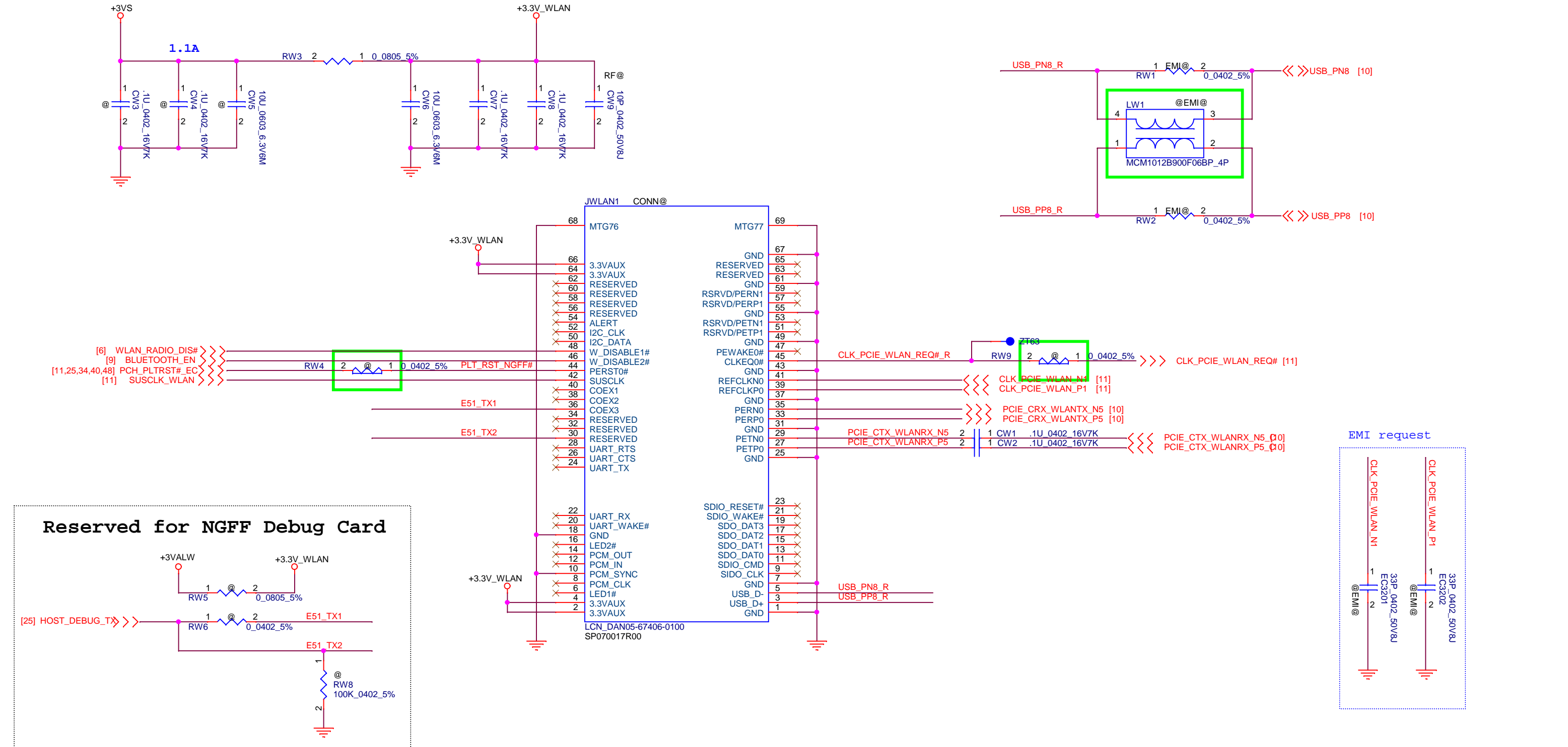


SOC TX
SOC RX



Pin	Signal
1	GND
2	A+
3	A-
4	GND
5	B-
6	B+
7	GND
8	DP
9	+5V
10	+5V
11	MD
12	GND
13	GND

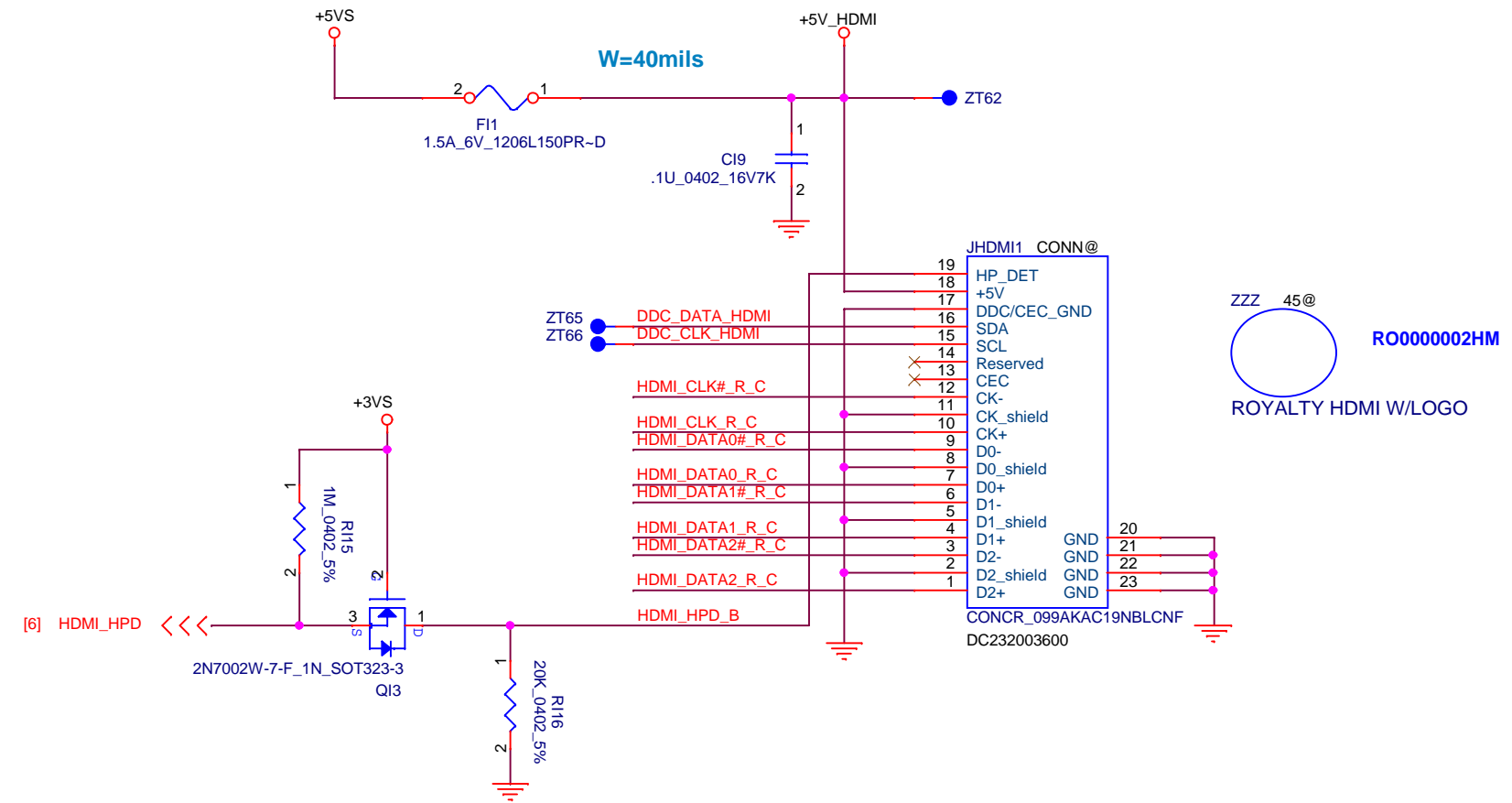
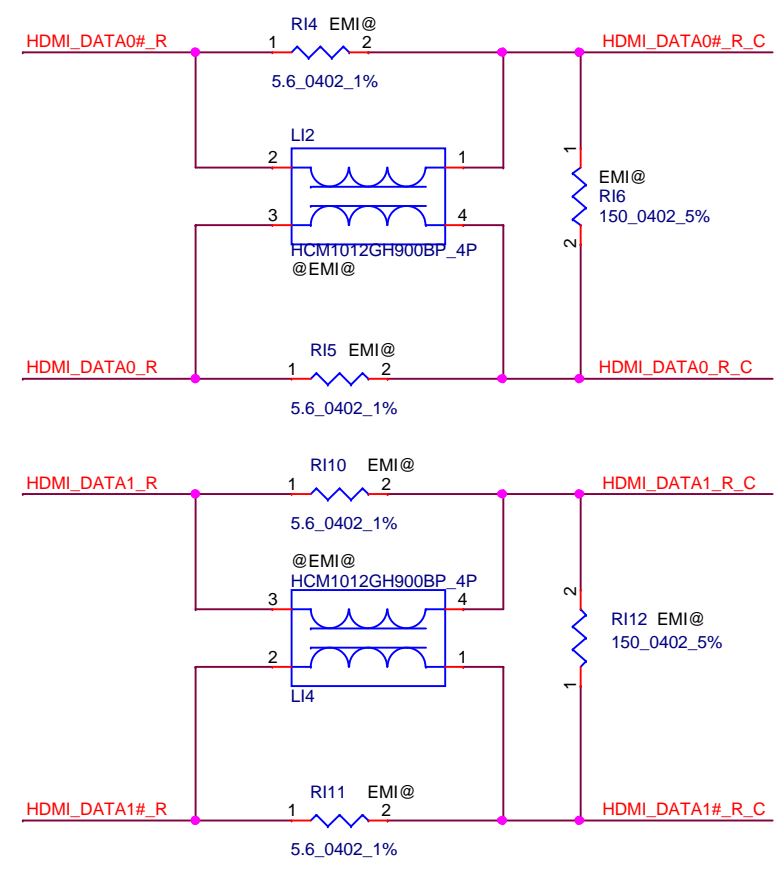
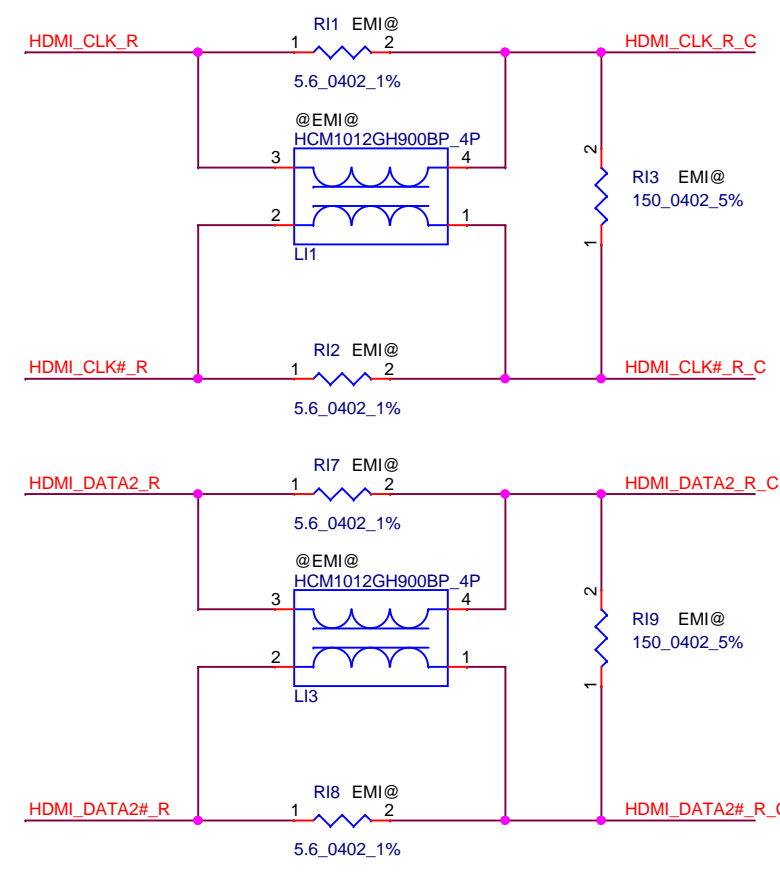
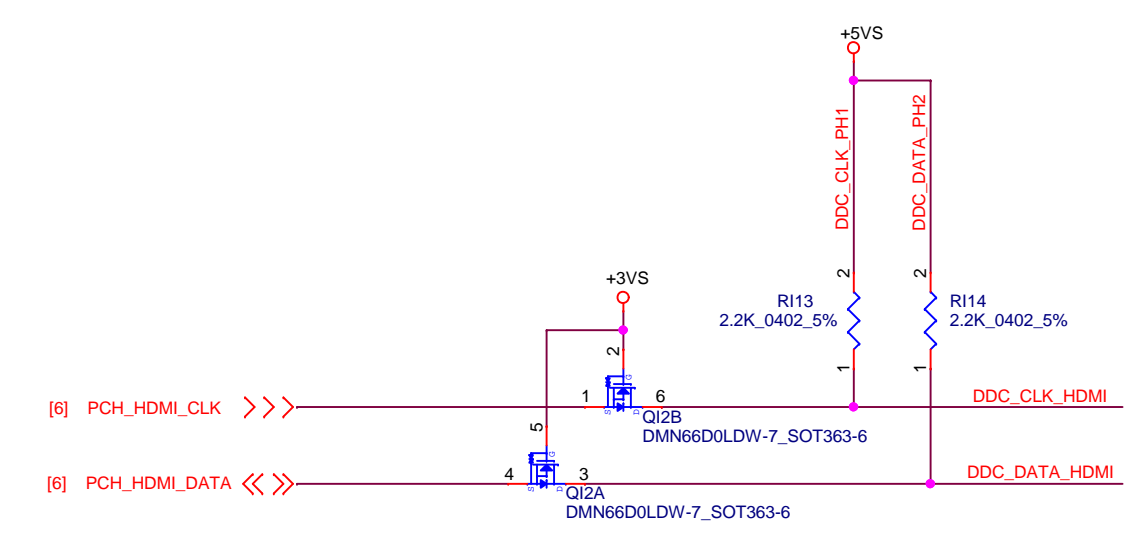
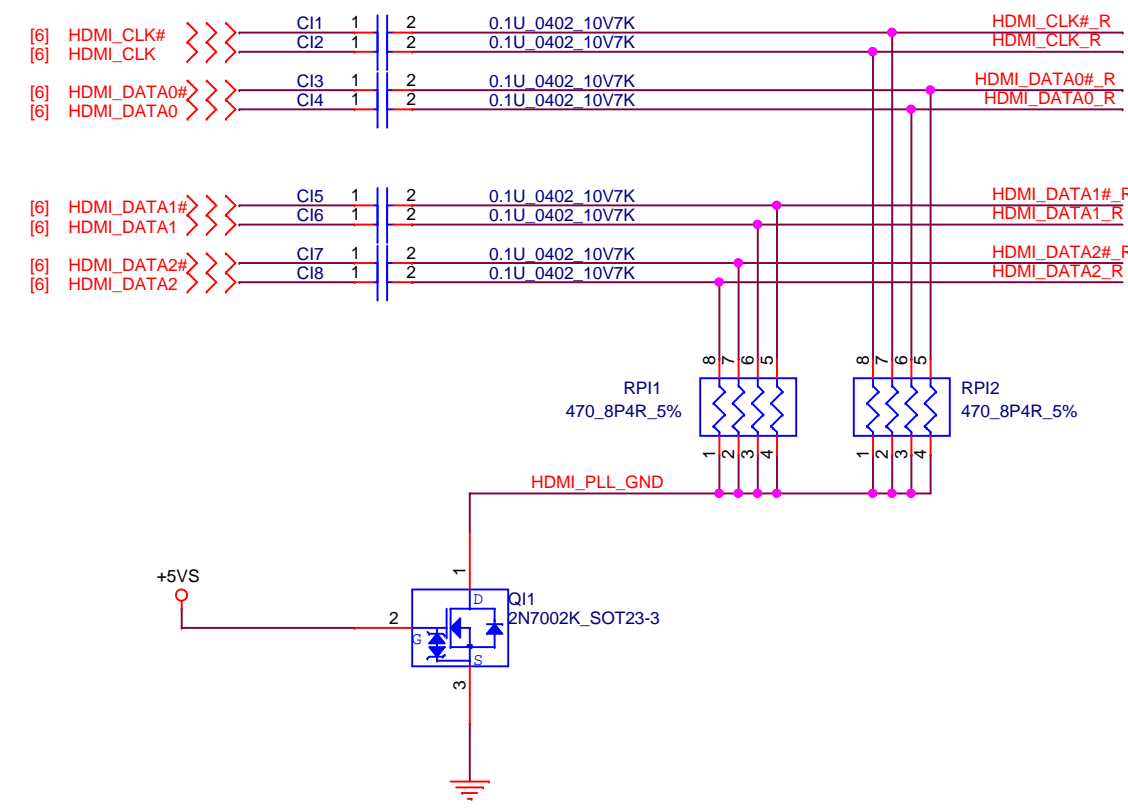
Main Func = WLAN A Key CONN



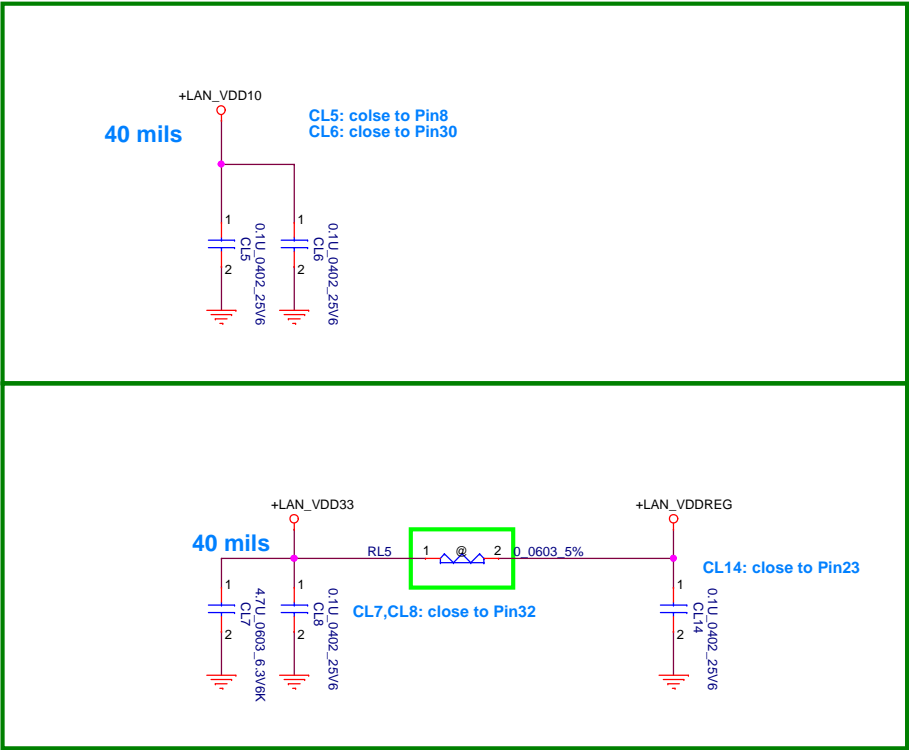
Support: Intel Dual Band Wireless-AC 3160

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Issued Date	2015/07/09	Deciphered Date	2016/07/31	Title	NGFF WLAN CONN
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				Rev	A00
				Date:	Tuesday, June 21, 2016
				Sheet	32 of 61

Main Func = HDMI

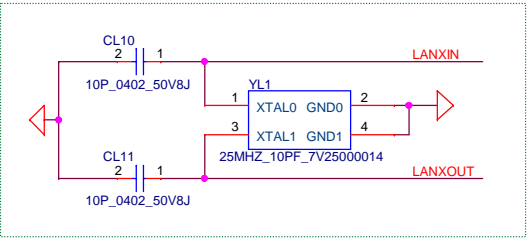


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2015/07/09	Deciphered Date	2016/07/31	Title		
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				Document Number	LA-D801P	
				Date	Tuesday, June 21, 2016	Rev A00
				Sheet	33	of 61

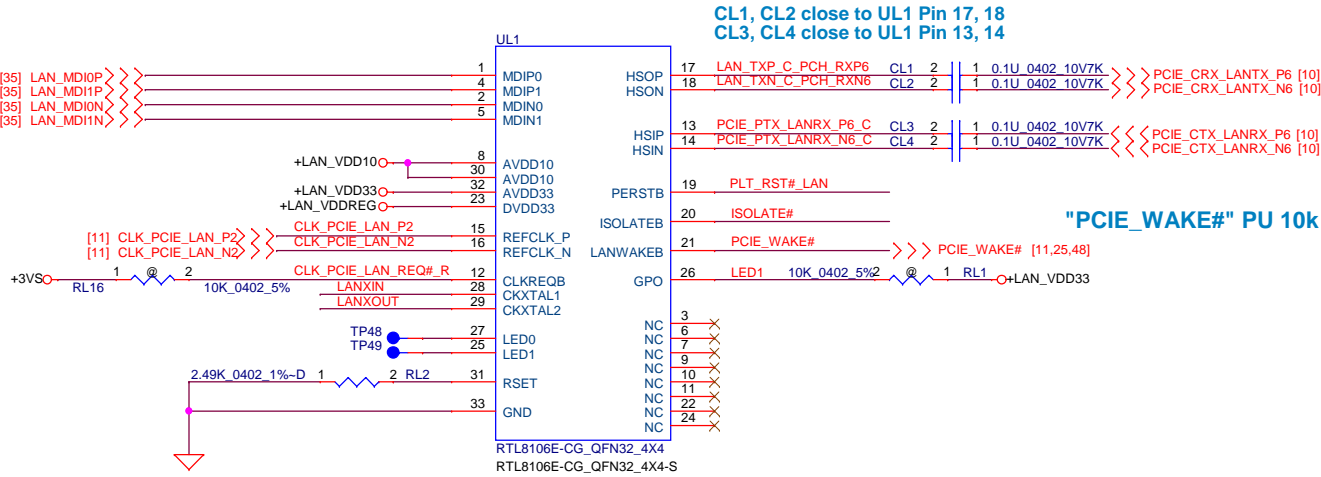


LAN CHIP 10/100M

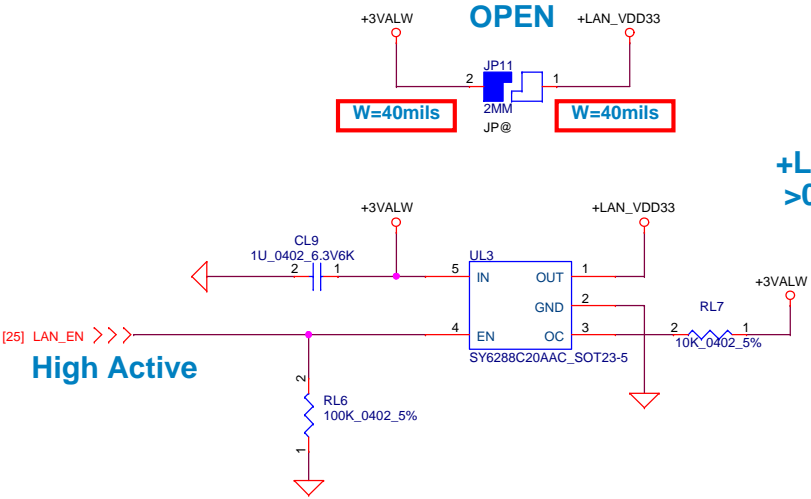
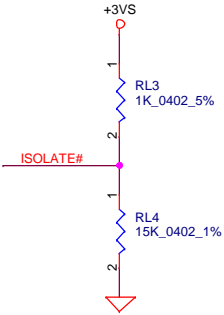
RTL8111GUS-CG	RTL8111G-CGT	RTL8106EUS-CG	RTL8106E-CG
			SA000065Y00
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M



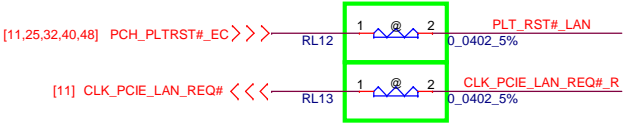
XTAL



"PCIE_WAKE#" PU 10k on EC side

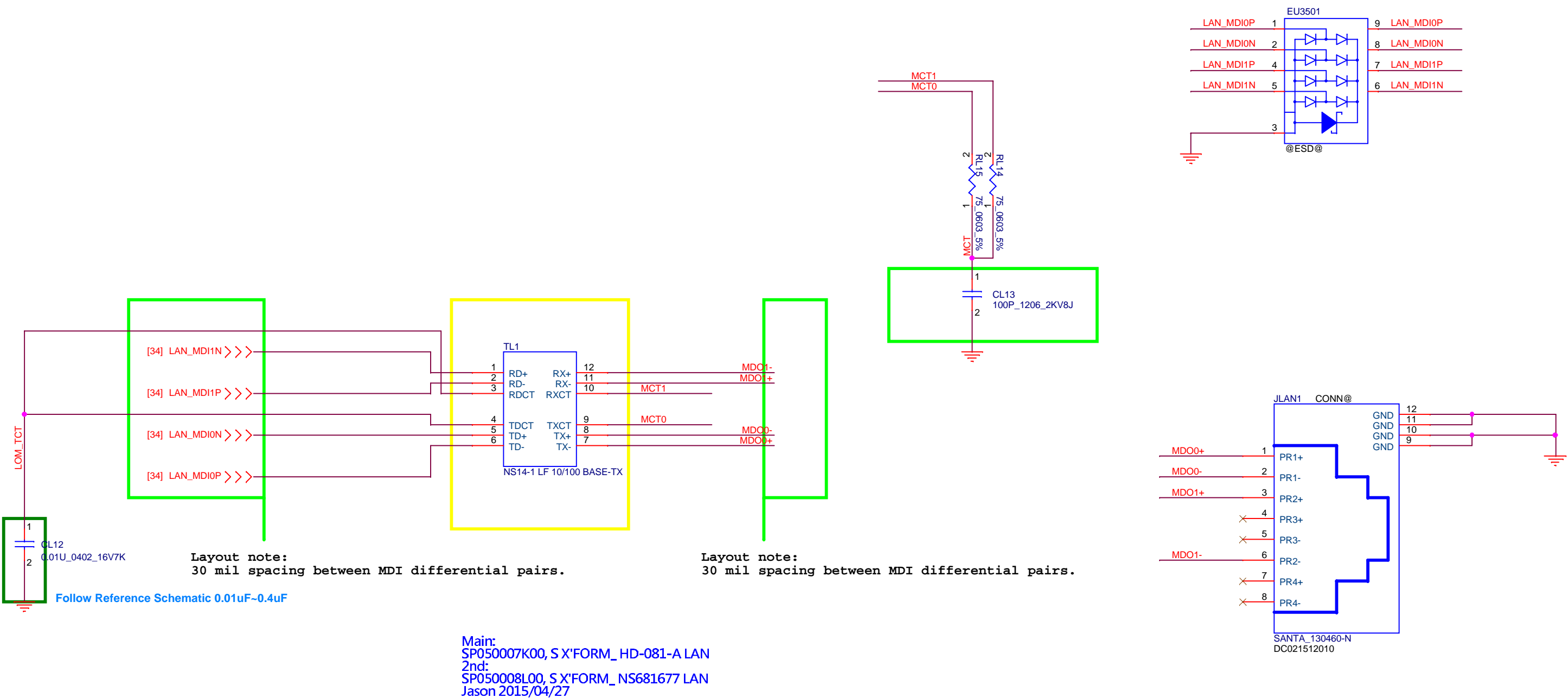


+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.

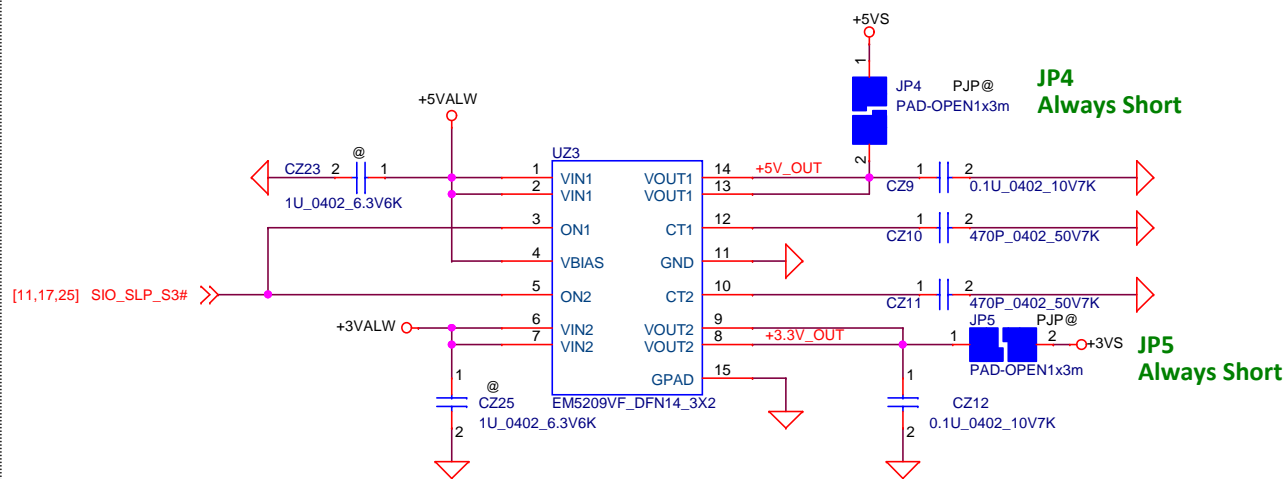


Main Func = LAN

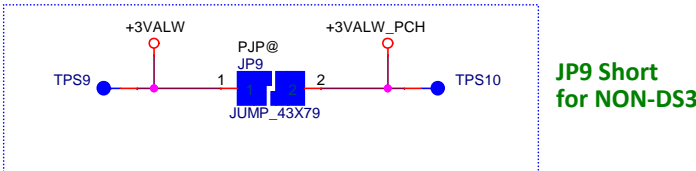
LAN TransFormer 10/100M



+5VS/+3VS for System



+3VALW_PCH for System



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

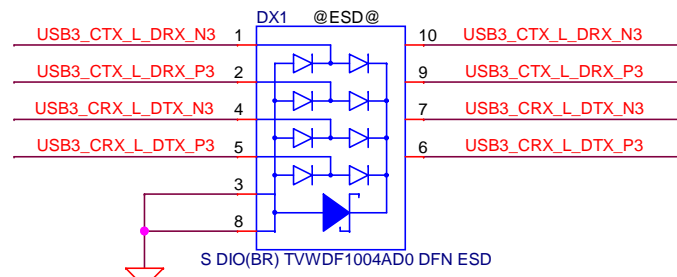
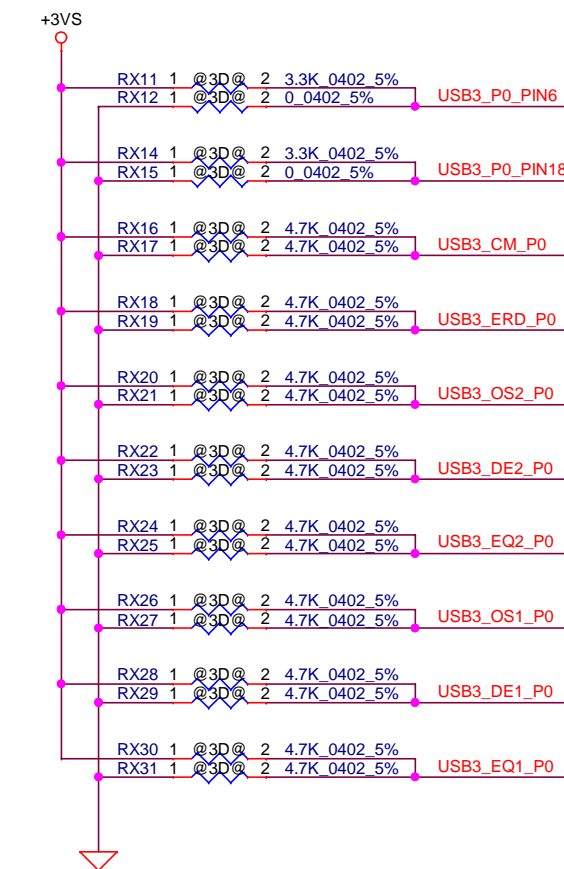
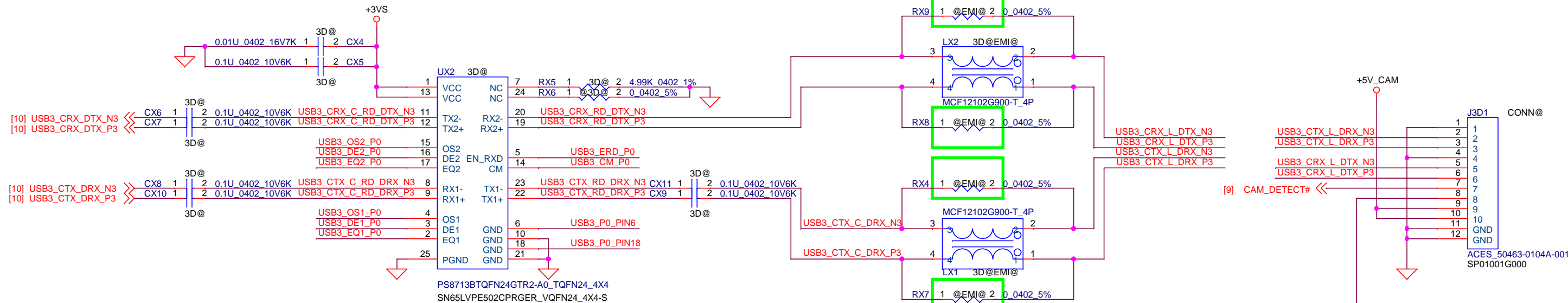
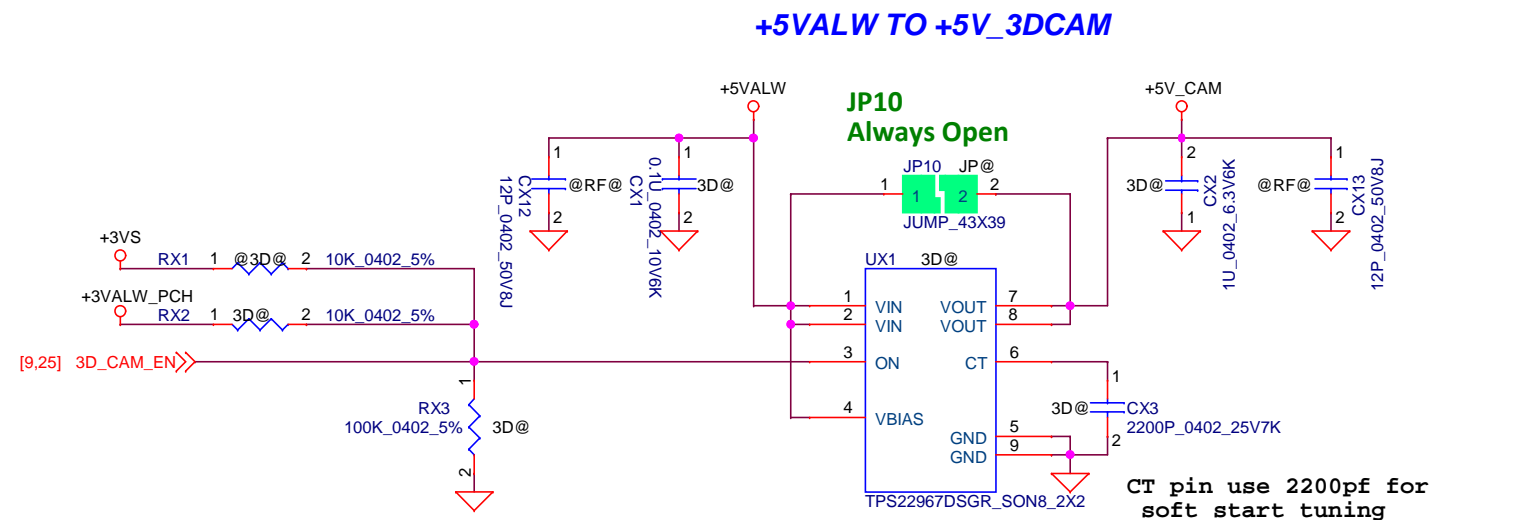
DC to DC

LA-D805P

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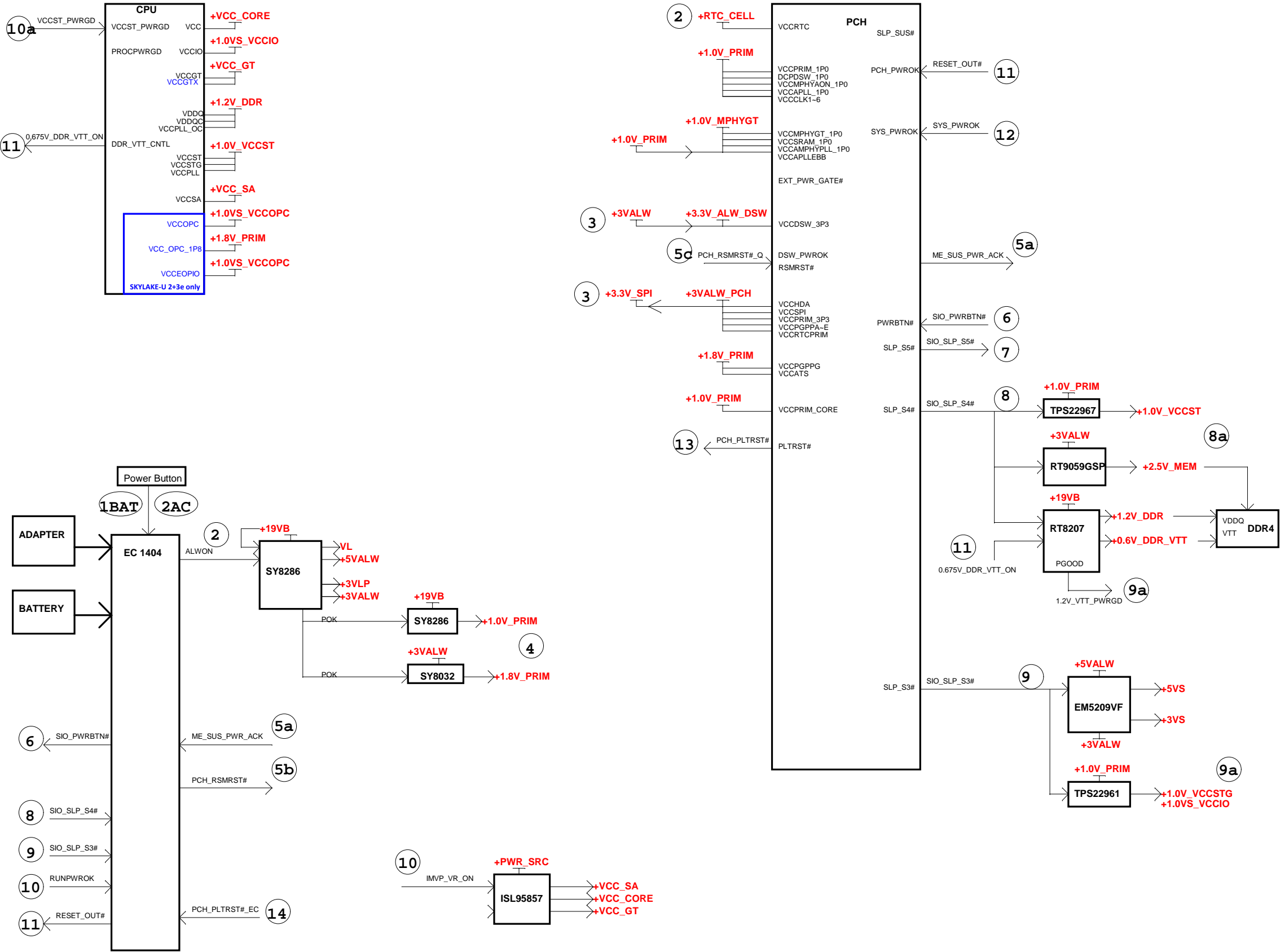
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Vendor	PS8713B	TI	Spec				schematic netname	3Vs	GND	
1	VDD	VCC	Same							
2	B_EQ0	EQ1	LL: 9.5dB (default)	LH: 13dB	HL: 4.5dB	HH: 7.7 dB	USB3_EQ1_P0	RI23	@	RI32 @
3	DE0	DE1	LL: 3.5dB (default)	LH: no DE	HL: 2.7dB	HH: 5 dB	USB3_DE1_P0	RI26	@	RI35 @
4	EQ1	OS1	LL: 9.5dB	LH: 13dB	HL: 4.5dB	HH: 7.7 dB	USB3_OS1_P0	RI22	@	RI40 @
5	PD#	EN_RXD	it can be left open				USB3_ERD_P0	RI44	@	RI48 @
6	B_DE1	GND	LL: 3.5dB (default)	LH: no DE	HL: 2.7dB	HH: 5 dB	USB3_P0_PIN6	RI53	@	RI49 @
7	REXT	NC	4.99K							RI56 4.99K
8	B_Inn	RX1-	Same							
9	B_Inp	RX1+	Same							
10	GND	GND	Same							
11	A_OUTn	TX2-	Same							
12	A_OUTp	TX2+	Same							
13	VDD	VCC	Same							
14	TST/NC	CM	4.7K ohm resistor for performance adjustment				USB3_CM_P0	RI42	@	RI46 @
15	A_EQ1	OS2	LL: 9.5 dB (default)	LH: 13 dB			USB3_OS2_P0	RI19	@	RI87 @
16	A_DE0	DE2	LL: 3.5dB (default)	LH: no DE	HL: 2.7dB	HH: 5 dB	USB3_DE2_P0	RI20	@	RI31 @
17	A_EQ0	EQ2	LL: 9.5 dB (default)	LH: 13 dB			USB3_EQ2_P0	RI21	@	RI36 @
18	A_DE1	GND	LL: 3.5dB (default)	LH: no DE	HL: 2.7dB	HH: 5 dB	USB3_P0_PIN18	RI52	@	RI50 @
19	A_Inp	RX2+	Same							
20	A_Inn	RX2-	Same							
21	GND	GND	Same							
22	B_OUTp	TX1+	Same							
23	B_OUTn	TX1-	Same							
24	I2C_EN	NC	this pin canbe NC or connected to GND				NC			RI57 @



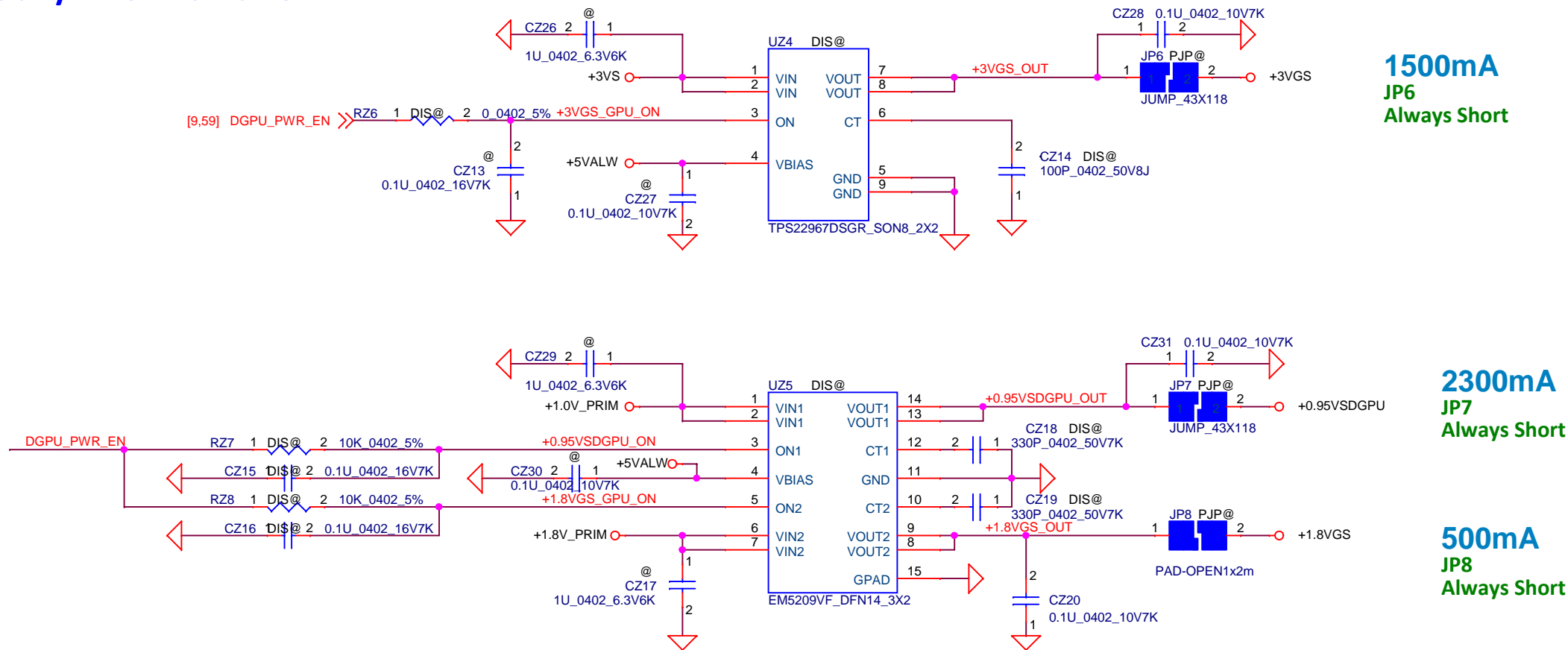
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2015/07/09	Deciphered Date	2016/07/31	Title	3D CAMERA
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Timing Diagram for S5 to S0 mode



DELL CONFIDENTIAL/PROPRIETARY

+3V/+0.95V/+1.8V for GPU



GPU R1/R3

UV1

SA000098V1L

M1_70_G5@

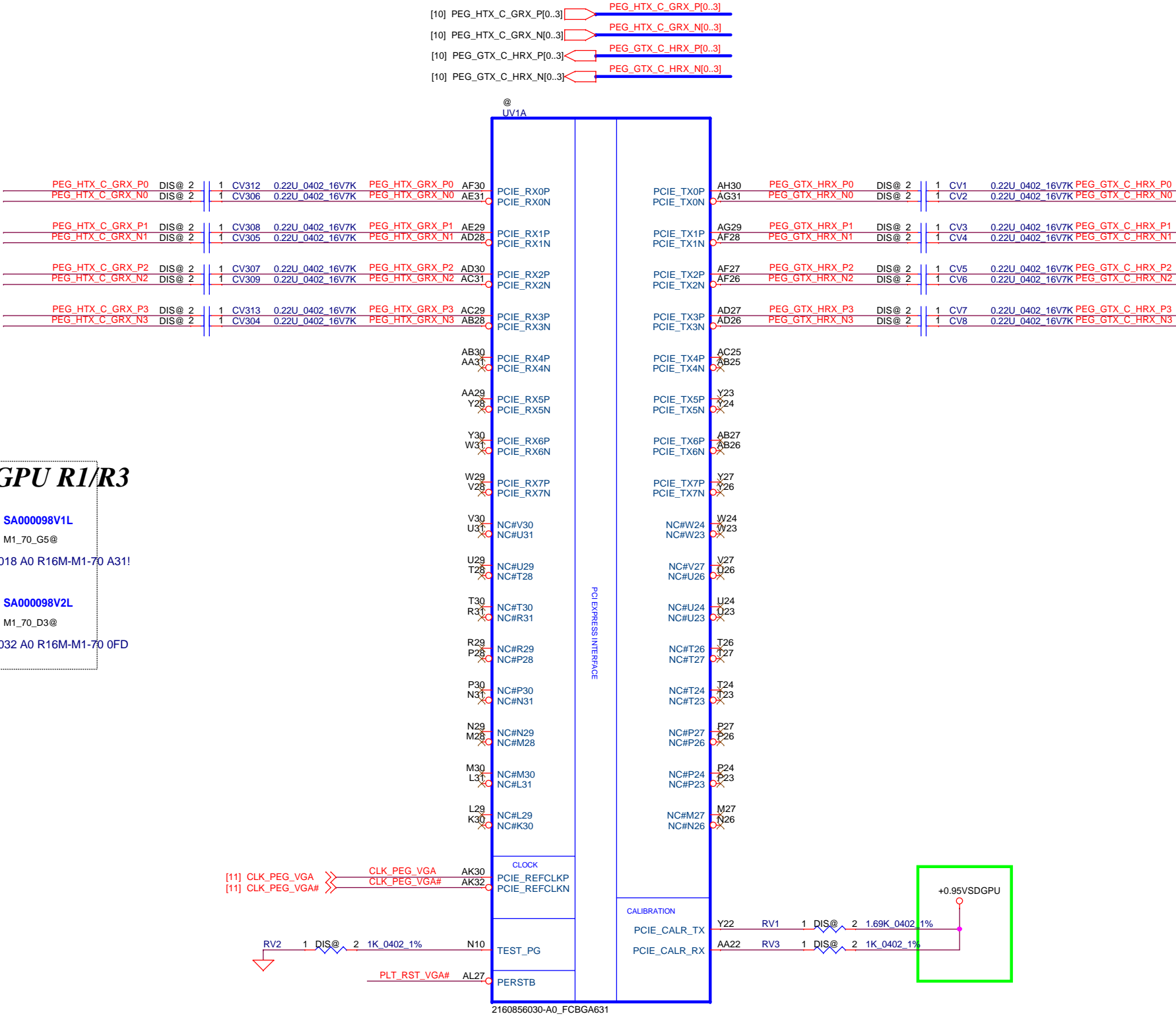
S IC 216-0889-018 A0 R16M-M1-70 A31!

UV1

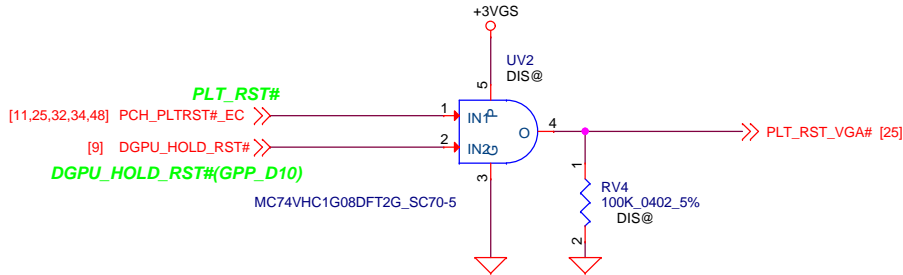
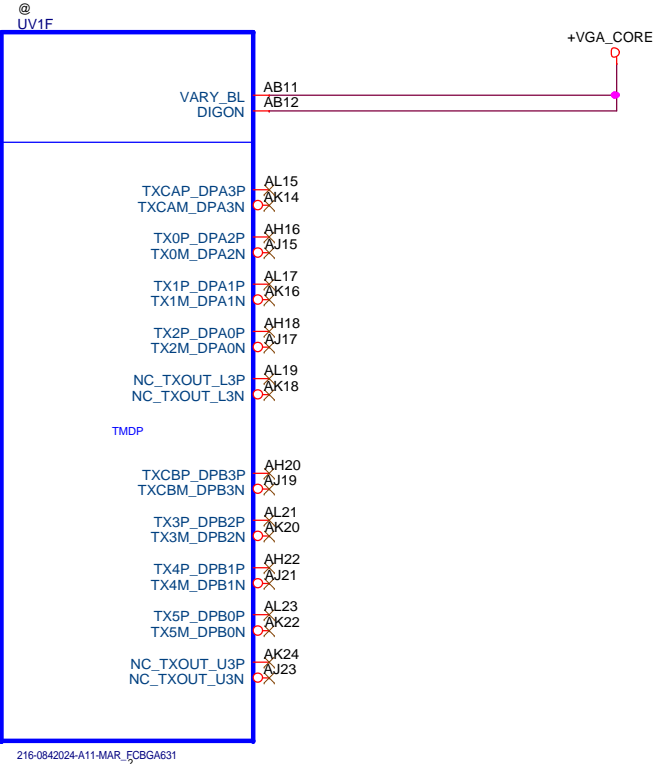
SA000098V2L

M1_70_D3@

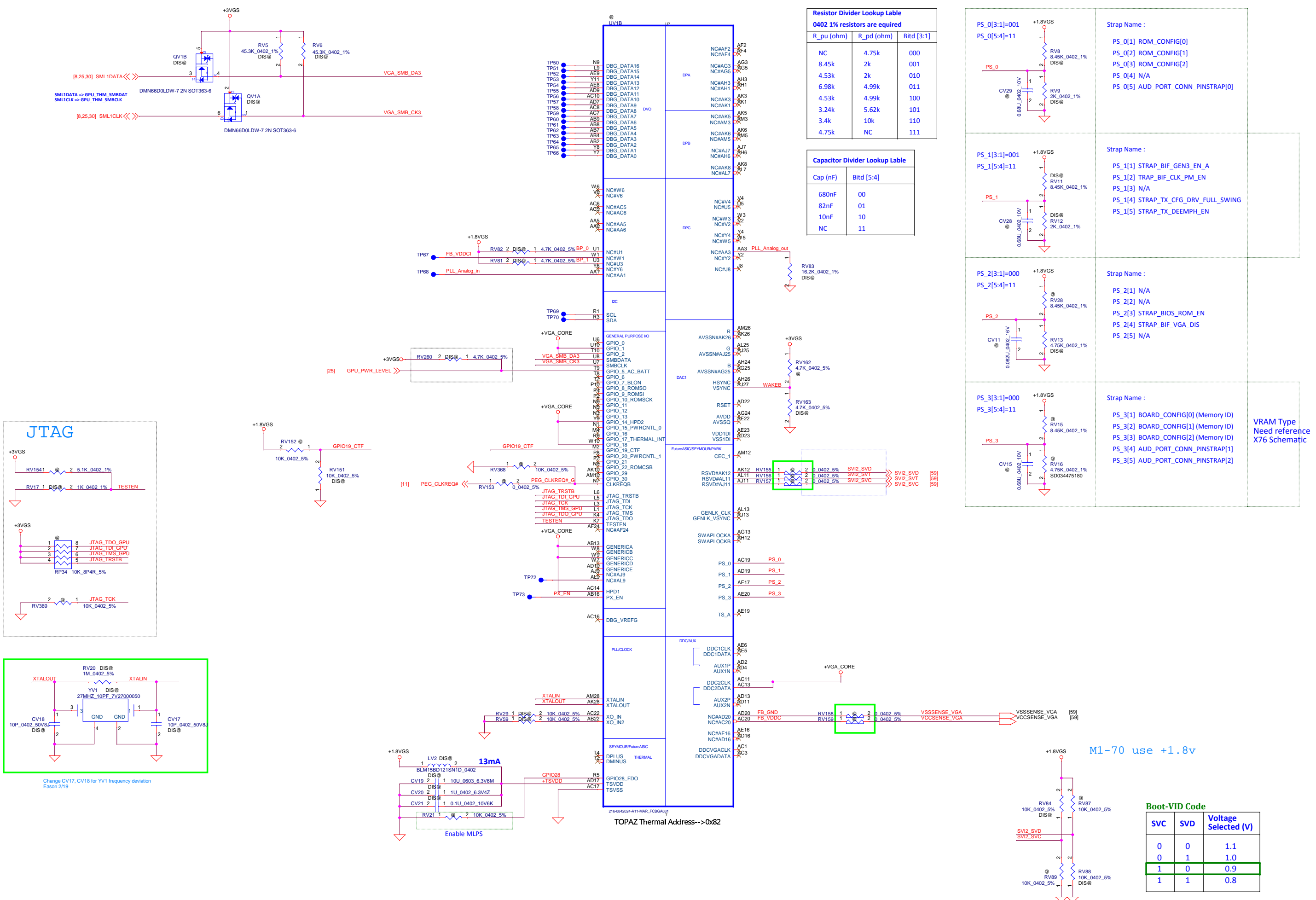
S IC 216-0864-032 A0 R16M-M1-70 0FD



No Use GPU Display Port output



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Issued Date	2015/07/09	Deciphered Date	2016/07/31	Title	MESO_(1/5)_PCIE/DP
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				Document Number	LA-D801P
				Date: Tuesday, June 21, 2016	Sheet 40 of 61



Resistor Divider Lookup Table			
0402 1% resistors are required			
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]	
NC	4.75k	000	
8.45k	2k	001	
4.53k	2k	010	
6.98k	4.99k	011	
4.53k	4.99k	100	
3.24k	5.62k	101	
3.4k	10k	110	
4.75k	NC	111	

Capacitor Divider Lookup Table		
Cap (nF)	Bitd [5:4]	
680nF	00	
82nF	01	
10nF	10	
NC	11	

PS_0[3:1]=001
PS_0[5:4]=11

Strap Name :

PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

PS_1[3:1]=001
PS_1[5:4]=11

Strap Name :

PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN

PS_2[3:1]=000
PS_2[5:4]=11

Strap Name :

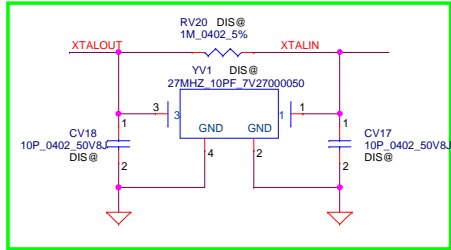
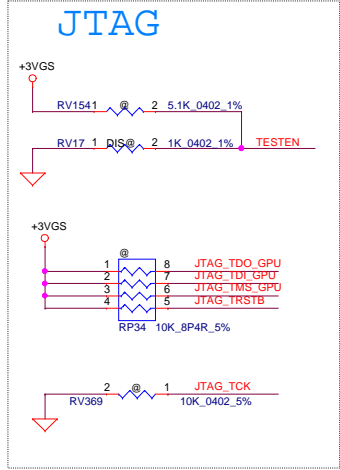
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A

PS_3[3:1]=000
PS_3[5:4]=11

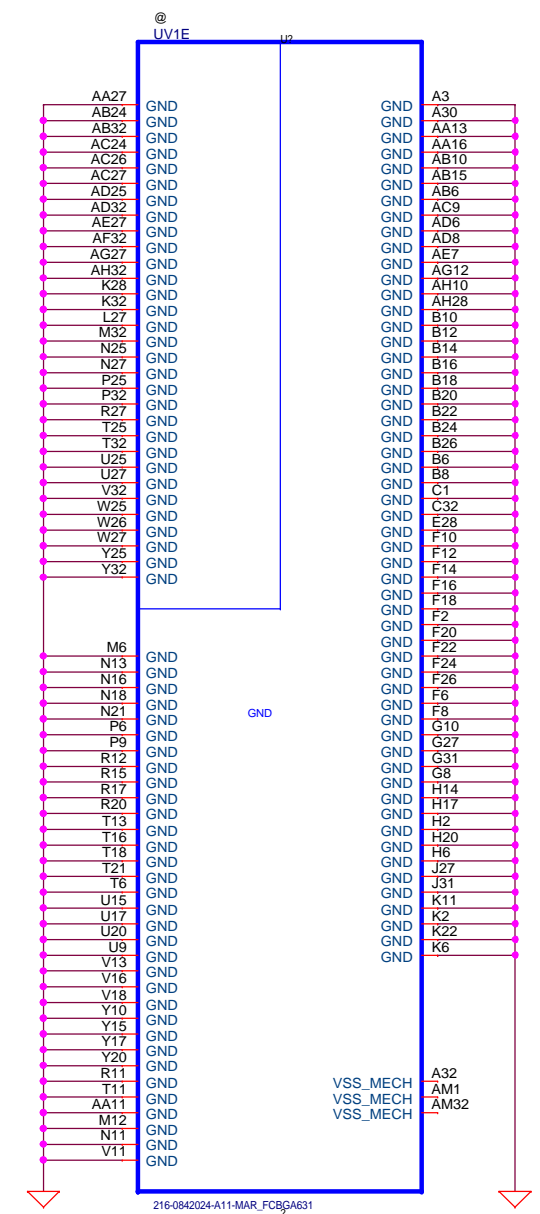
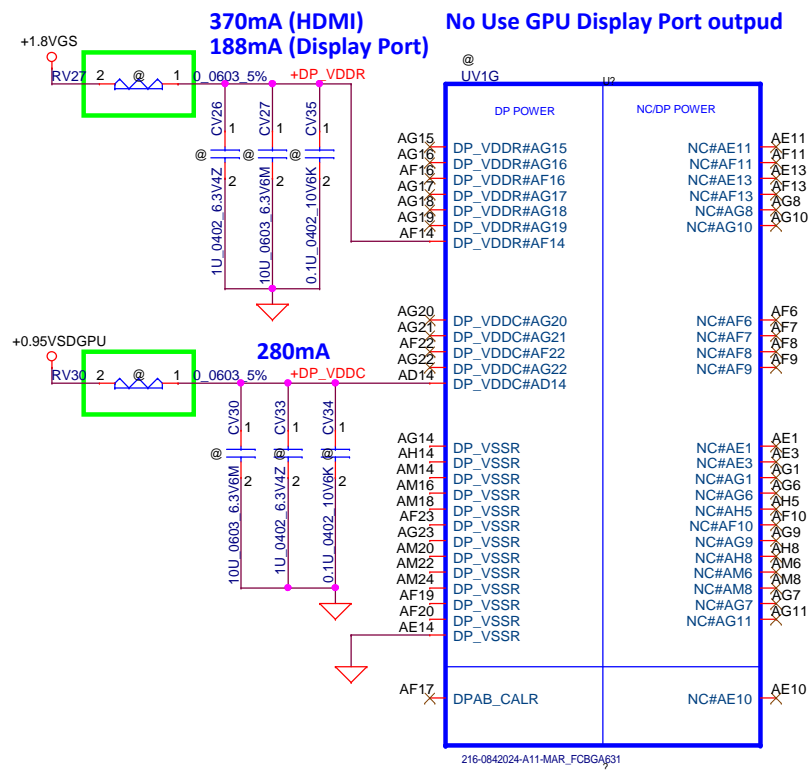
Strap Name :

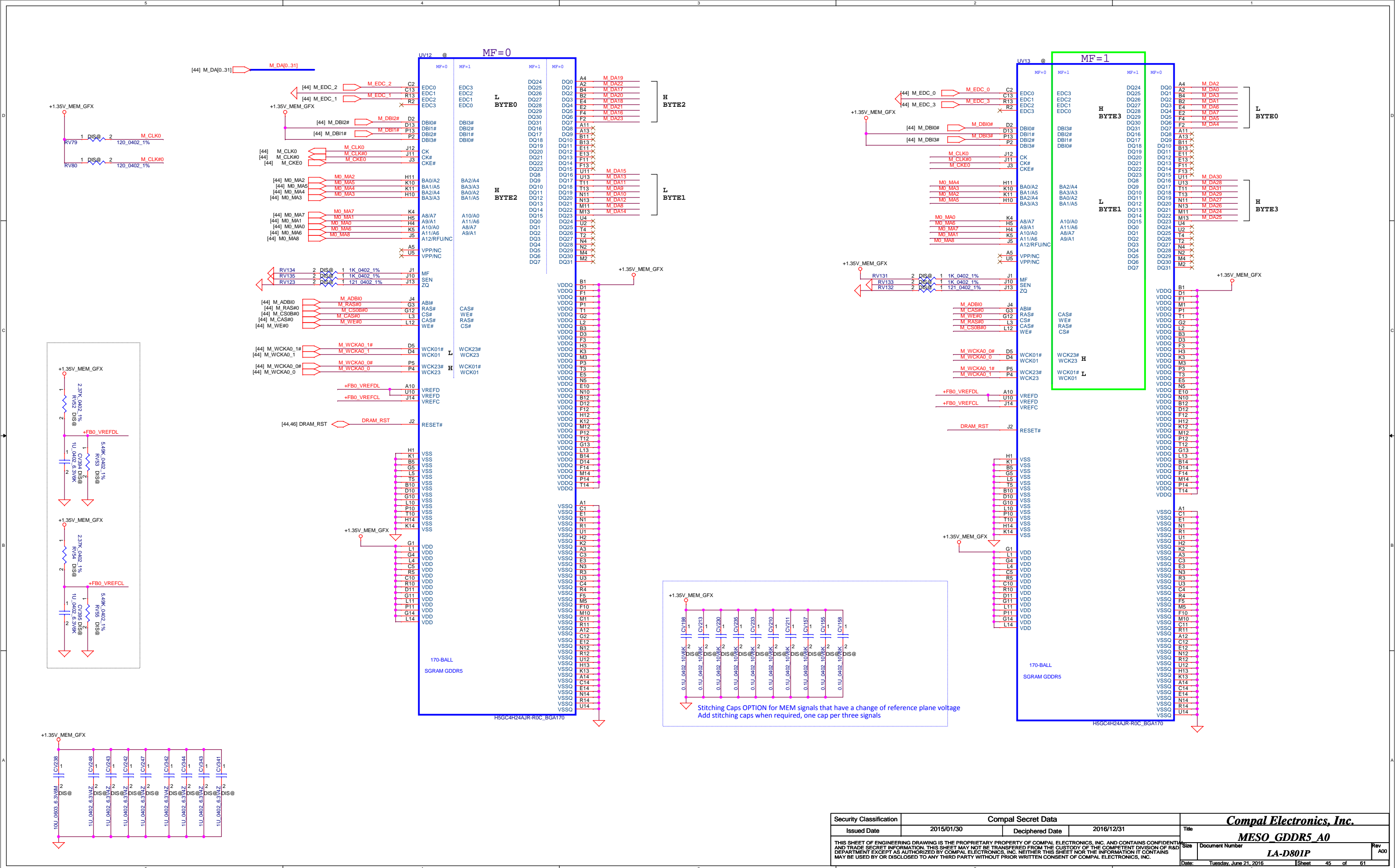
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

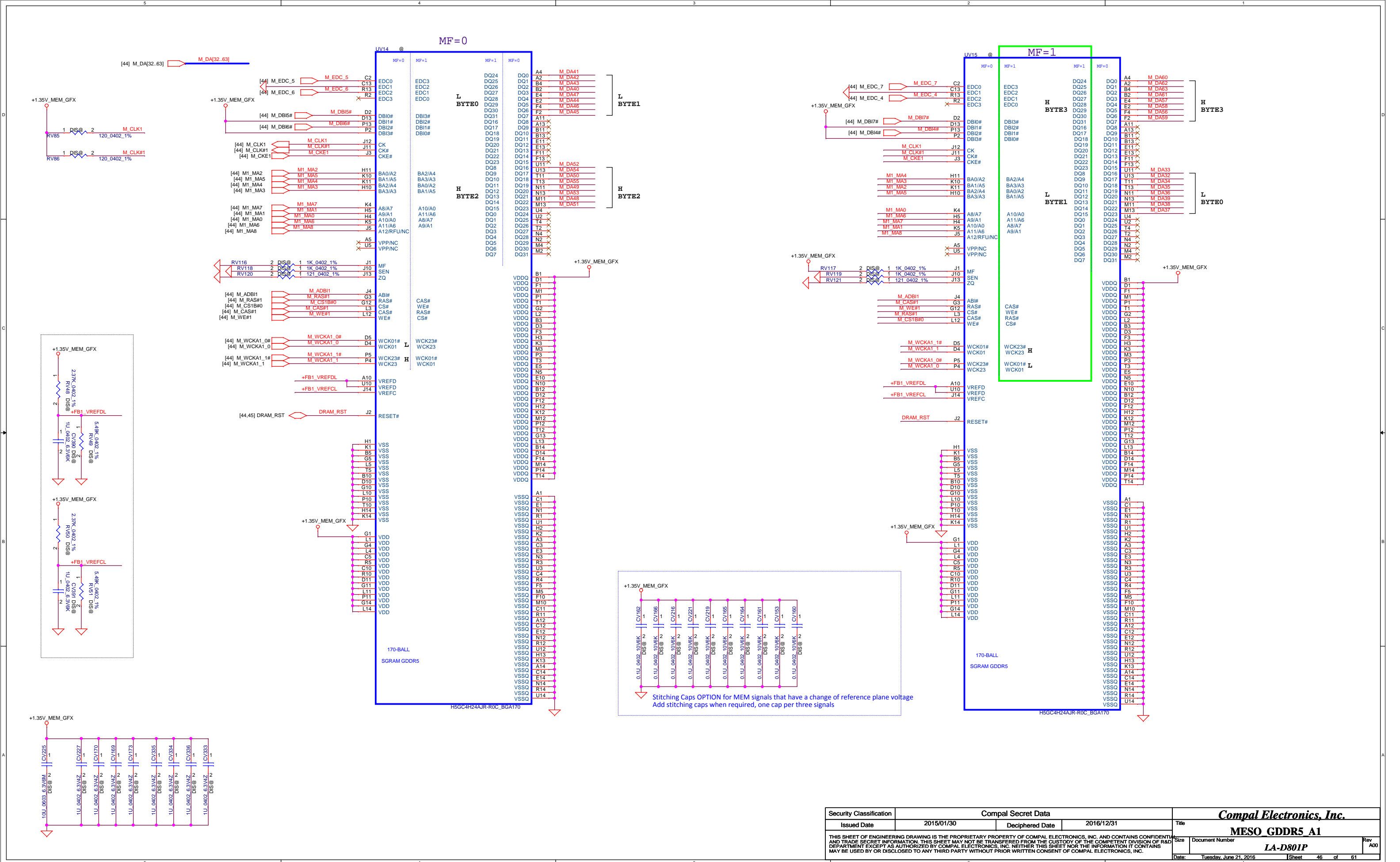
VRAM Type
Need reference
X76 Schematic



Change CV17, CV18 for YV1 frequency deviation
Eason 2/19

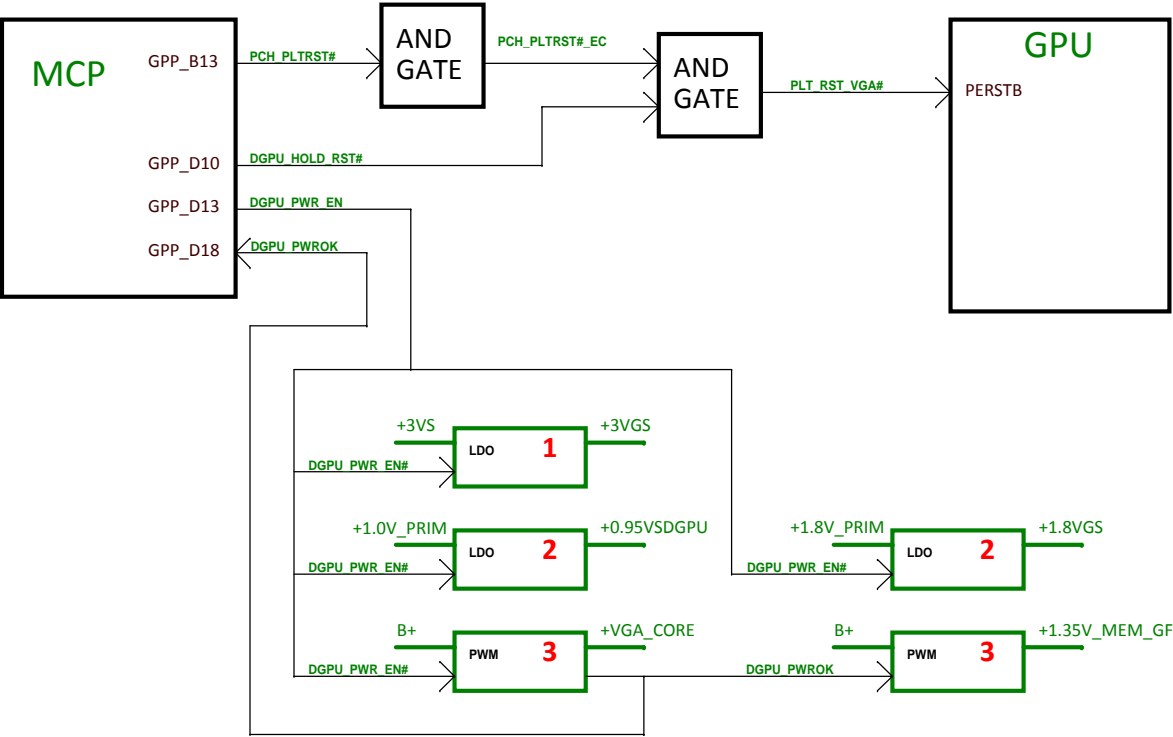
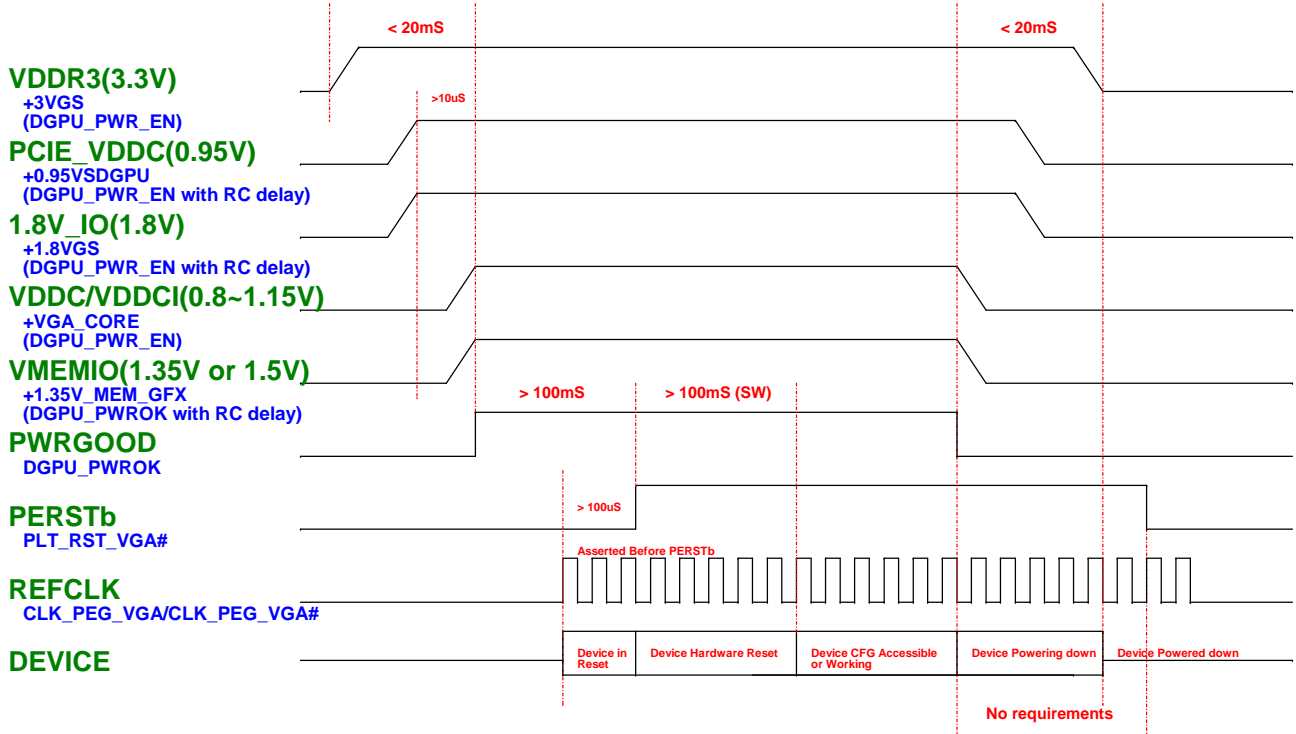




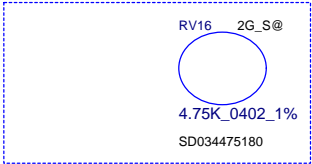


Power-Up/Down Sequence

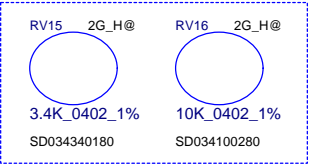
1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
2. It is recommended that the 3.3-V rail ramp up first.
3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.
4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress? idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ? 50 mV/μs).
5. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
6. For power down, reversing the ramp-up sequence is recommended.



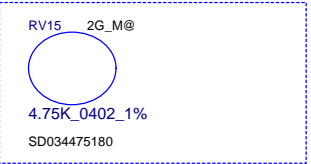
Samsung 2G



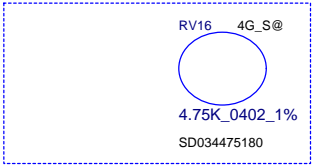
Hynix 2G



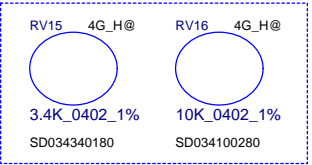
Micron 2G



Samsung 4G



Hynix 4G



Micron 4G

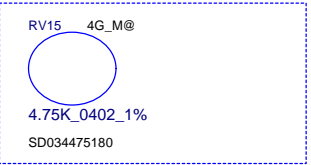


Table 3–21 Resistor Divider Lookup T.

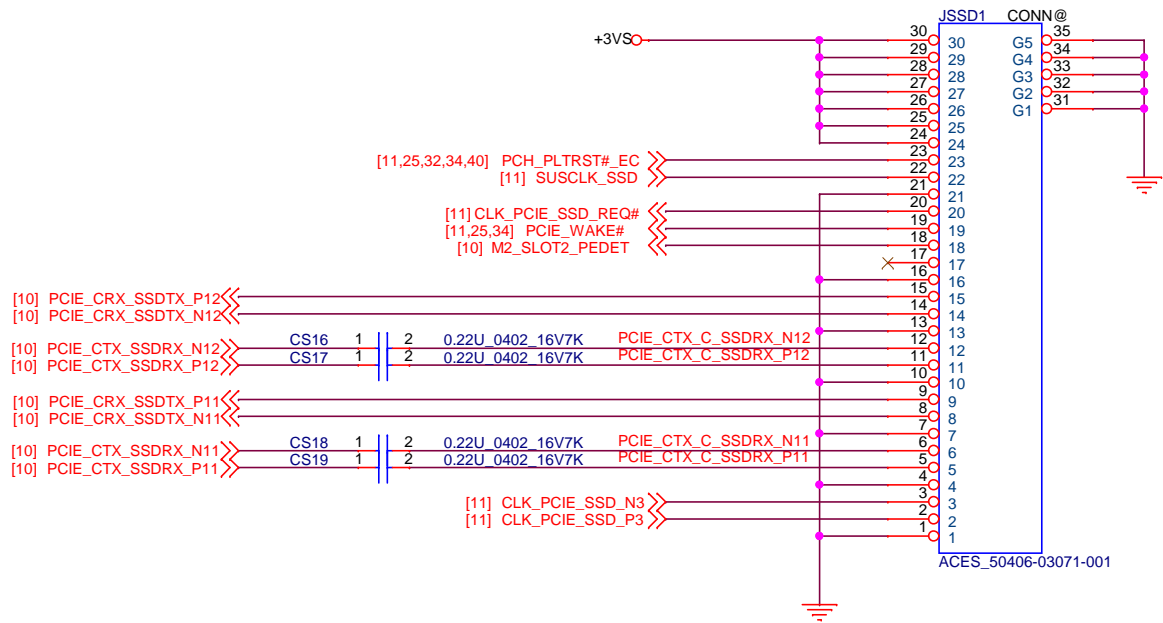
R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

For AMD R16M-M1-70 VRAM Only

Memory ID	4Gb R3 P/N	Vendor	Configuration	Size
000	SA00009TT1L	SAMSUNG	S IC D5 128M32 K4G41325FE-HC28 FBGA A31!	2GB
110	SA00008HQ1L	Hynix	S IC D5 128M32/3G H5GC4H24AJR-R0C A31!	2GB
111	SA00009E31L	Micron	S IC D5 128M32 EDW4032BABG-70-F-R A31!	2GB

Memory ID	8Gb R3 P/N	Vendor	Configuration	Size
000	SA000092D1L	SAMSUNG	S IC D5 256M32 K4G80325FB-HC28 FBGA A31!	4GB
110	SA00009U11L	Hynix	S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!	4GB
111	SA00009TV1L	Micron	S IC D5 256M32 MT51J256M32HF-70:A A31!	4GB



"M2_SLOT2_PEDET" PU 10k on DB

PEDET	Module Type
0	SATA
1	PCIE

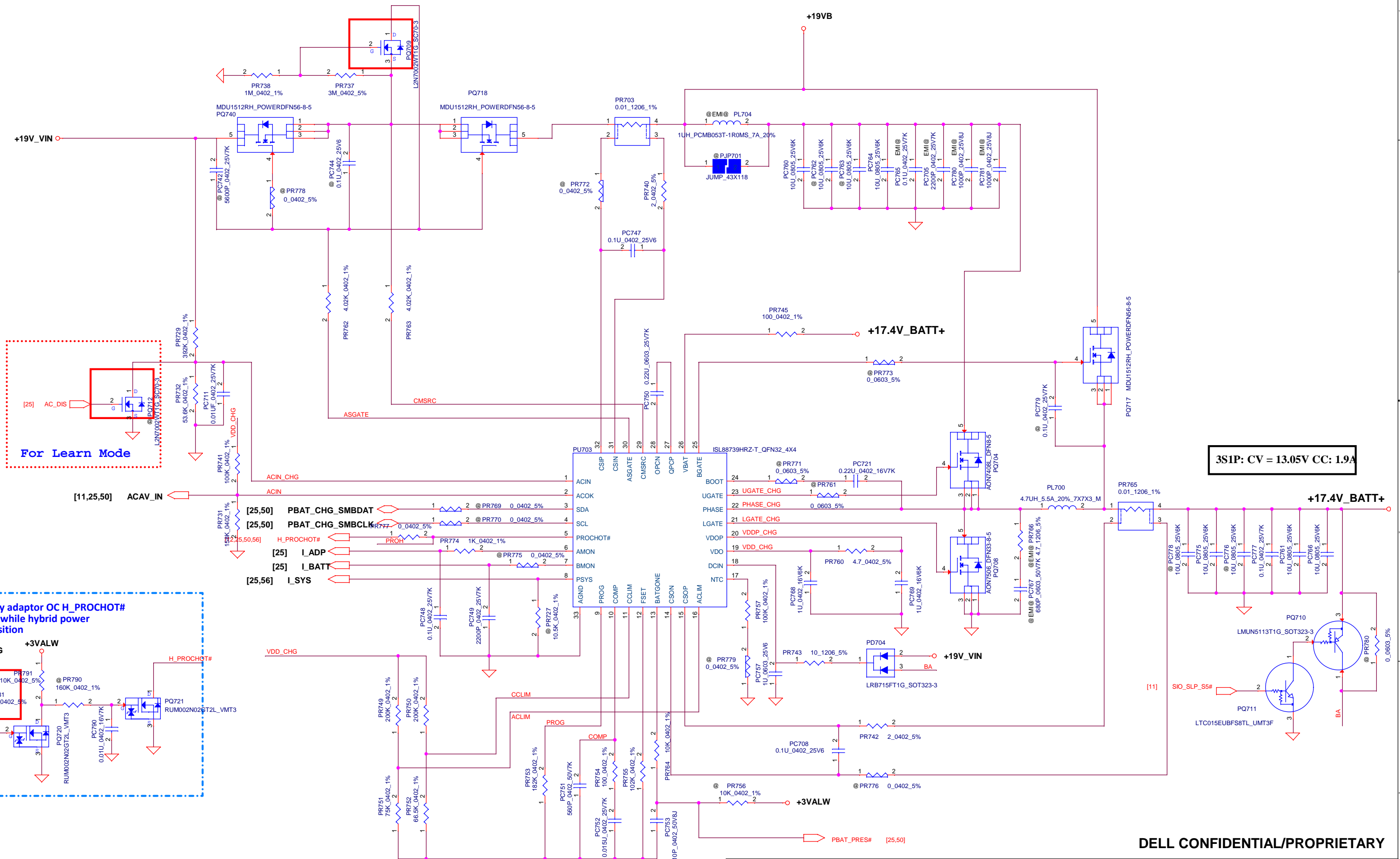
Version Change List (P. I. R. List)

1	Design Change					
2	Item	Date	Page	Part reference	change description	Reason
3	Based on LA-D801P_0106					
4	1	2016/1/8	20	CD29	Change CD29 Pin1 Net from "H_DRAMRST#" to "DDR4_DRAMRST#"	Modify DDR4_DRAMRST# Sequence
5	2	2016/1/8	20, 21	CD27,CD57	Change CD27,CD57 Footprint	Material change, D7 H1.1 --> D2 H1.9
6	3	2016/1/8	22	H8,H9,H10,H11,H13	Modify H8,H9,H10,H11, Add H13	ME change
7	4	2016/1/8	22	TP27,TP28,TP29	Add TP27,TP28,TP29	CPU Test point
8	5	2016/1/14	22	U1,C17,R57	Change U1,C17, Add R57	Change to Stand Part
9	6	2016/1/20	9	JWDB1,RC190,RC191	Add JWDB1,RC190,RC191	Add Win7 Debug
10	7	2016/2/2	39	CZ20	Change CZ20 Pin1 Net from "+1.8VGS" to "+1.8VGS_OUT"	Layout
11	8	2016/2/2	18	L1,L2	Change L1,L2 Footprint	Material change, sourcer request
12	9	2016/2/2	30	F3	Change F3 Footprint	Material change, sourcer request
13	10	2016/3/2	18	OC61	Change OC61 Pin1 Net from "+3.3V_HDA" to "+3VALW_PCH"	follow RF test result
14	11	2016/3/2	18	OC82	Change OC82 Pin1 Net from "+1.0V_APLL" to "+1.0V_PRIM"	follow RF test result
15	12	2016/3/2	48	JSSD1	Swap SSD Pin define and cancel "SSD_DEVSLP"	For cable wiring methods
16	13	2016/3/4	35	JLAN1	JLAN1.9 --> LANGND1 JLAN1.10 --> LANGND1 JLAN1.11 --> LANGND2 JLAN1.12 --> LANGND2	HI-POT modify
					CL13.2 --> LANGND2	
17	14	2016/3/8	25, 28	UEI.113,RE64,D4.3	UEI.113 add 0 ohm then connect to D4.3	Modify LCD BITS Sequence
18	15	2016/3/10	33	RP12,LL2	HDMI_CLK#_R --> HDMI_CLK_R HDMI_DATA0#_R --> HDMI_DATA0_R HDMI_DATA0#_R_C --> HDMI_DATA0_R_C	HDMI signal Layout modify, EMI request
19	16	2016/3/16	17, 36, 39	CZ21,CZ22,CZ23,CZ24,CZ25,CZ26,CZ27,CZ28,CZ29,CZ30,CZ31	Add Capacitance close to Vin, Vbias, Vout, CT	Load Switch common design
20	17	2016/3/16	9	RC190,RC191	Add RC190,RC191 connect to GPP_A22	VRAM ID
21	18	2016/3/18	35	JLAN1	JLAN1.9 --> GND JLAN1.10 --> GND JLAN1.11 --> GND JLAN1.12 --> GND CL13.2 --> GND	HI-POT modify
22	19	2016/3/21	11, 17	DZ4,DZ5,RZ9,RC192	Reserve DZ4,DZ5,RZ9,RC192	Speed up SLP_S3# & SLP_S3# power down sequence
23	20	2016/3/22	29	JPWR1	Change JPWR1 Footprint	ME request
24	21	2016/3/22	48	JSSD1	PCIE_CRX_SSDTX_P12 --> PCIE_CRX_SSDTX_P11 PCIE_CRX_SSDTX_N12 --> PCIE_CRX_SSDTX_N11 PCIE_CTX_SSDRX_N12 --> PCIE_CTX_SSDRX_N11 PCIE_CTX_SSDRX_P12 --> PCIE_CTX_SSDRX_P11 PCIE_CTX_C_SSDRX_N12 --> PCIE_CTX_C_SSDRX_N11 PCIE_CTX_C_SSDRX_P12 --> PCIE_CTX_C_SSDRX_P11	For cable wiring methods
25	22	2016/3/22	20	CD29	Change CD29 BOM Config to @	SAMMANG DRAM issue
26	DVT2					
27	23	2016/4/22	25	UEI.30	Change LED control signal net name from "SATA_LED#_R" to "SATA_LED_EN"	EC request
28	24	2016/4/22	29	JPWR1	Change Footprint	ME request
29	25	2016/4/25	22	H6	Φ5 --> Φ5.6	ME request
30	26	2016/4/25	24	RA36,RA37	Change footprint from Bead to Resistance	EMI request
31	27	2016/4/25	45	UV3,UV4,UV5,UV6	Change footprint from "MT41J128M16TT-093_FBGGA_96P_A39" to "MT41J256M16LY-091G-N_FBGGA_96P"	DFB request, LA-D805P only
32	28	2016/5/3	29	JPWR1	Change Footprint, E-T_6915K-Q06N-00L --> JXT_FP226H-006S1BEM	ME request
33	29	2016/5/3	12	OC89	Add "1pF_0402" on "HDA_RST#"	RF request
34	Pilot					
35	30	2016/5/5	18	L2	Change Footprint, BLM15BD601CN1D --> LQGH5HS4N7502D	RF request
36	31	2016/5/9		RA1,RA22,RW3,R51	Change Footprint from "R_0805" to "R0805_0ohm"	Change to Short PAD
37				RA4,RA39,RC17,RC161,RC1	Change Footprint from "R_0603" to "R0603_0ohm"	
38				RA2,RA5,RA17,RA18,RA6,F	Change Footprint from "R_0402" to "R0402_0ohm"	
39	32	2016/5/10		RB45,RE22,RE28,RE37,RE38	Change Footprint from "R_0402" to "R0402_0ohm"	Change to Short PAD
40	33	2016/5/20		LW1,L4	Change Footprint from "INPAQ_MCM1012B900F06BP_4P" to "INPAQ_MCM1012B900F06BP_4P"	Close solder mask
41	34	2016/5/20		LU2,LU3,LU5,LU6	Change Footprint from "INPAQ_HCM1012GH900BP_4P" to "INPAQ_HCM1012GH900BP_4P-NP1"	Close solder mask
42	35	2016/5/20		RU1,RU2,RX4,RX7,RU7,RX	Change Footprint from "R_0402" to "R0402-NPM"	Close solder mask
43	36	2016/5/20	30	JKB1	Change Footprint from "ACES_50699-03041-P01_30P" to "STARC_132C30-100020-A2-R_30P"	DFB request
44	37	2016/5/30	11	RC81	Del RC81	For Layout optimally
45	38	2016/6/13	33	LI1,LI2,LI3,LI4	Change Footprint from "INPAQ_HCM1012GH900BP_4P" to "INPAQ_HCM1012GH900BP_4P-NP1"	Close solder mask
46	39	2016/6/15	7	OC90	Add OC90	Reserve for fine-tune +0.6V_DDR_VTT sequence
47	40	2016/6/15		RC75,RE45	Change Footprint from "R0402_0ohm" to "R_0402"	Change to 0 Ohm
48	41	2016/6/15		RW3	Change Footprint from "R0805_0ohm" to "R_0805"	Reserve for BT lose issue
49	42	2016/6/15		RW5	Change Footprint from "R_0402" to "R_0805"	

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						X00
				Date: Tuesday, June 21, 2016	Sheet 50 of 61	

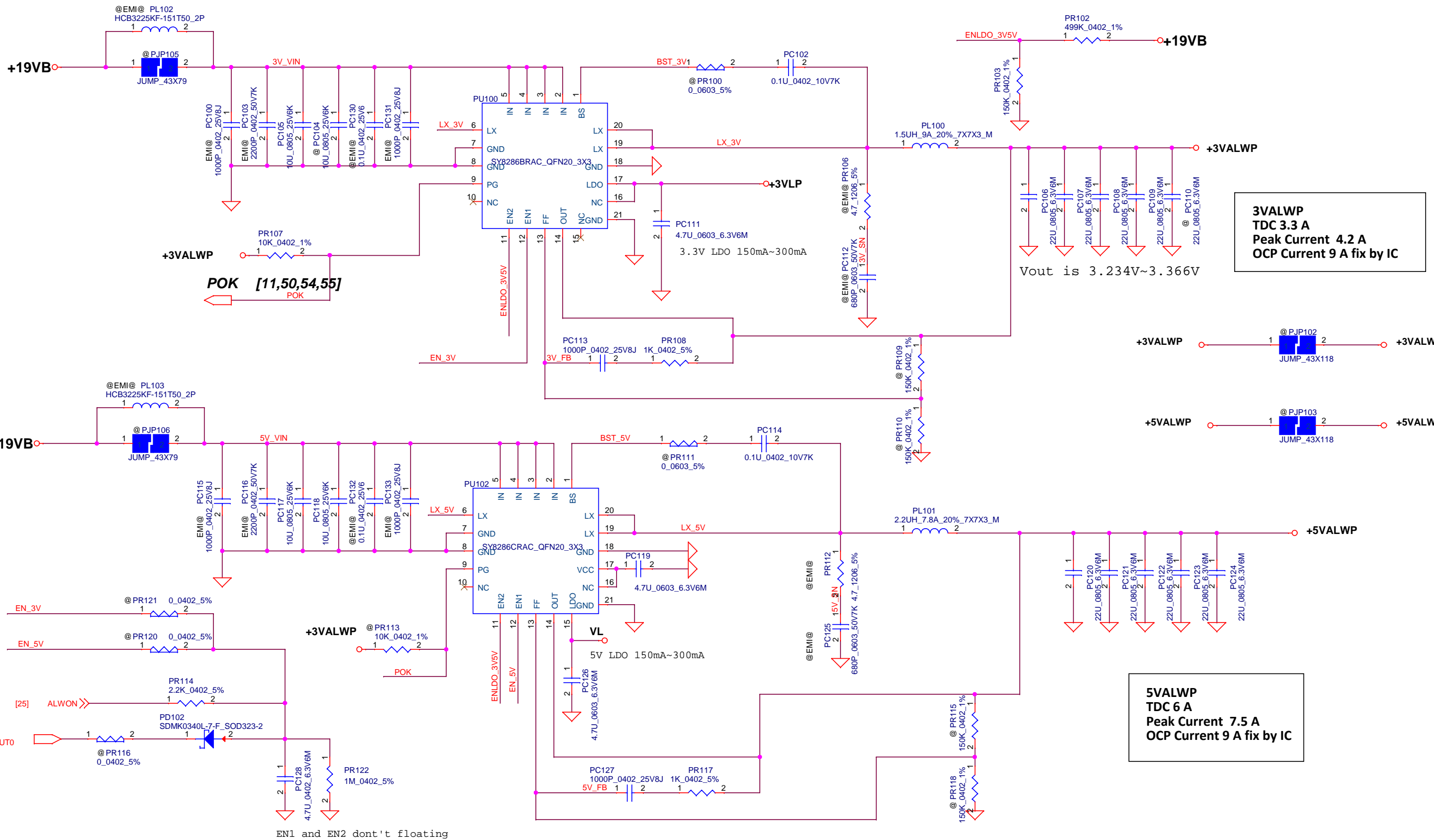
I_{ada}=0~2.30A(45W)

$$ADP_I = 32 \cdot I_{\text{adapter}} \cdot R_{\text{sense}}$$



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				Date:	Tuesday, June 21, 2016	Sheet 51 of 61

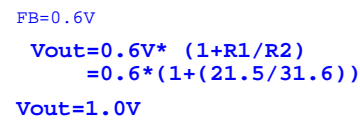


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Compal Electronics, Inc.			
Title			
PWR_3.3VALWP/5VALWP			
Size	Document Number		Rev
	LA-D801P		X00
Date:	Tuesday, June 21, 2016		Sheet 52 of 61

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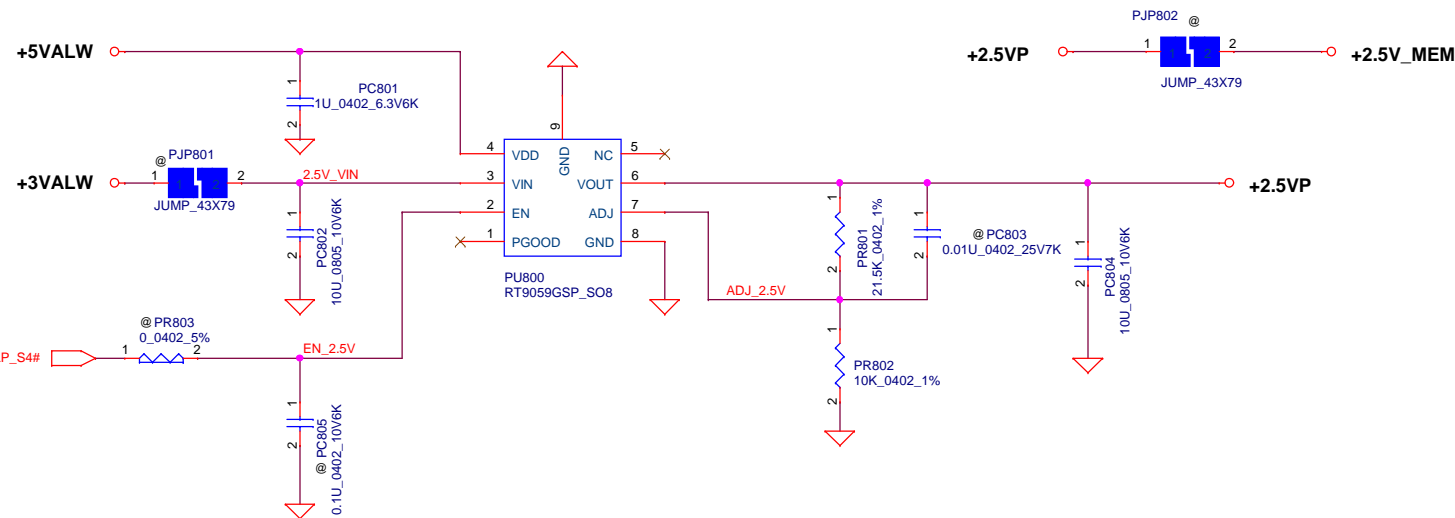
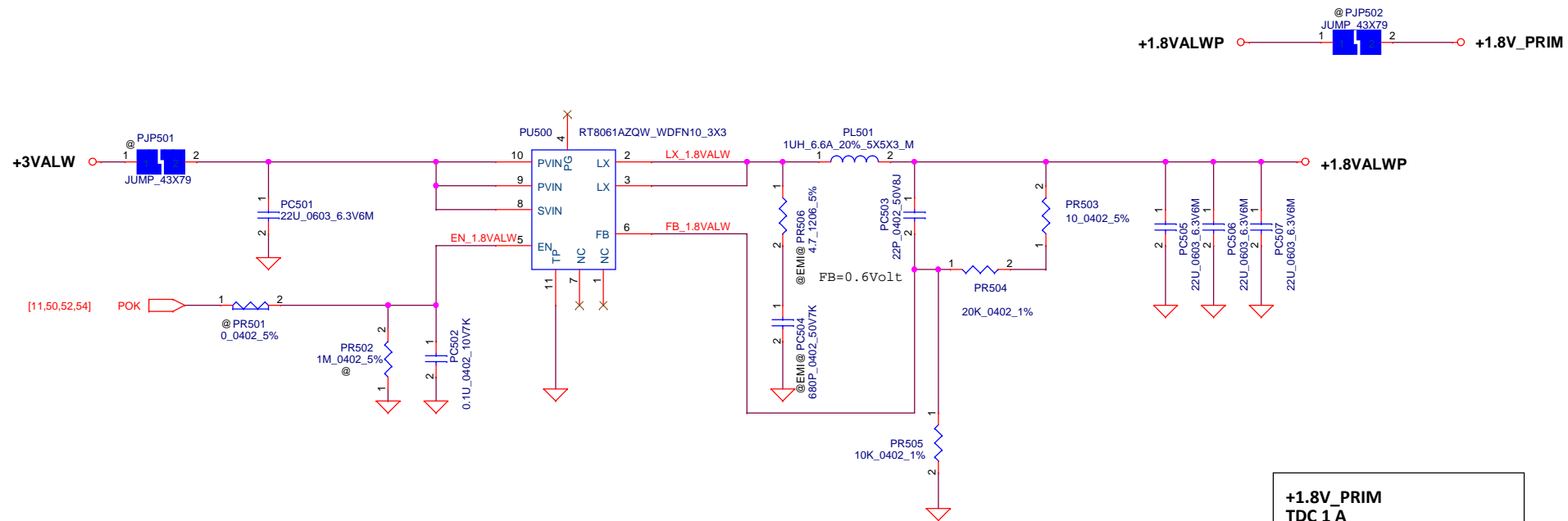
Security Classification	Compal Secret Data					
Issued Date	2015/03/23	Deciphered Date	2014/12/15	Title PWR_+1.2V_MEN/+0.6V_DDR_VTT		
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				Custom		X00
Date: Tuesday, June 21, 2016				Sheet	53	of 61



+1.0V_PRIM
TDC 6 A
Peak Current 8.6 A
OCP Current 12 A Fix by IC
Choke DCR 11.0mohm , 12.0mohm

OCp setting	ILMT(pin3)
6A	Pull low
9A	Floating
12A	Pull high

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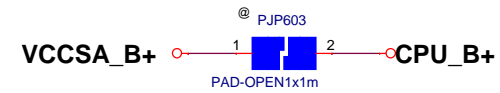
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/03/23	Deciphered Date	2014/12/15	Title	PWR +1.8V PRIM and +2.5V
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				Date: Tuesday, June 21, 2016	Sheet 55 of 61

Local sense put on HW site

+1.0V_VCCST

VCC_SA
Loadline : 10.3m-ohm

TDC 5A
Peak Current 5A
OCP current 7A
Choke DCR 12 +-5% ohm



VCCSA_B+

+3VS

+5VALW

ISL95859HRTZ-T_TQFN40_5X5

+5VALW

+VCC_SA

+5VALW

	U22@SKL	U22@KBL
PR640	255	280
PR648	1.37K	1.5K
PR629	84.5K	97.6K

PR640 U22@KBL@

PR648 U22@KBL@

PR629 U22@KBL@

Local sense put on HW site

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						Size	Document Number			Rev	
						Date:	Tuesday, June 21, 2016		Sheet	56	of

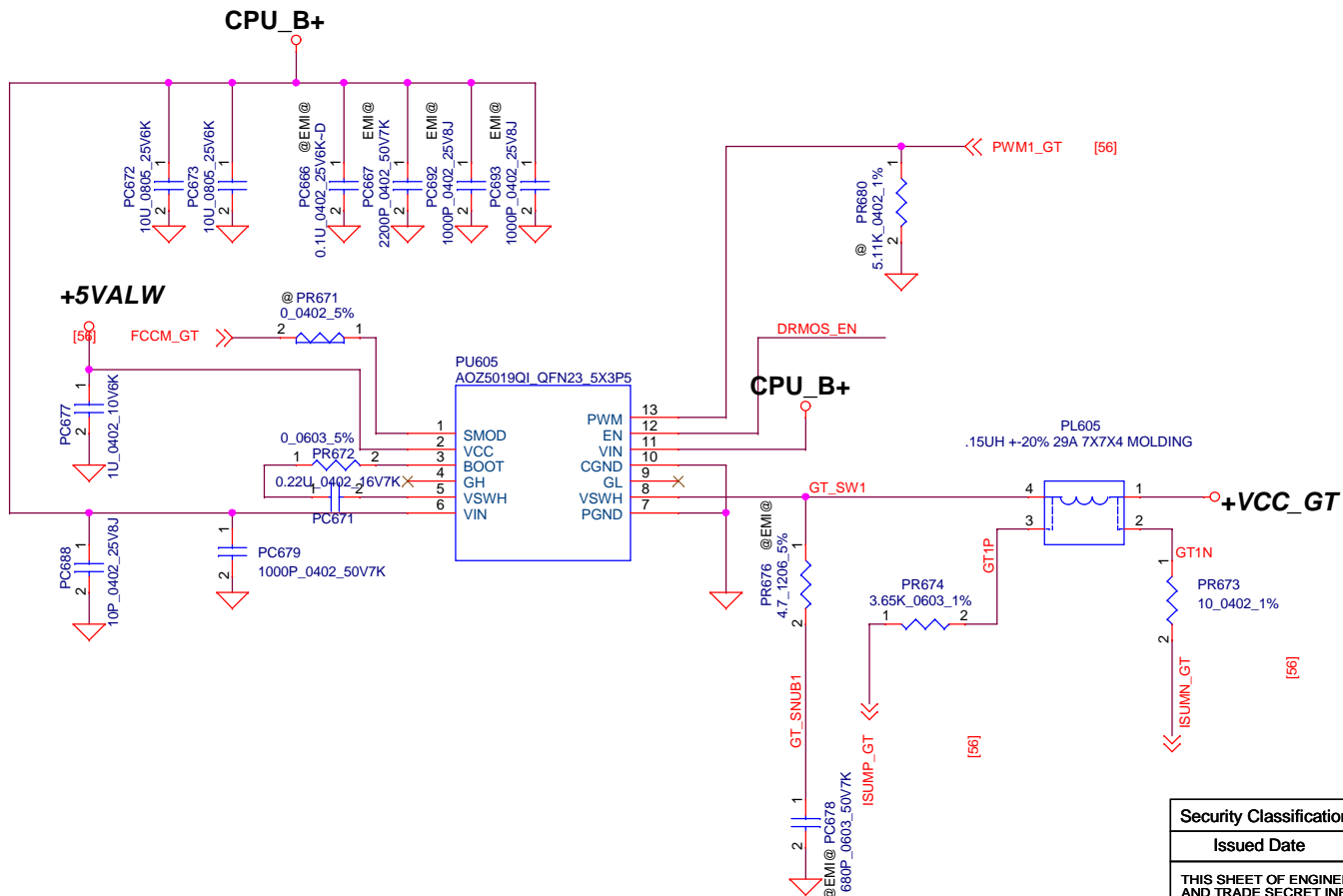
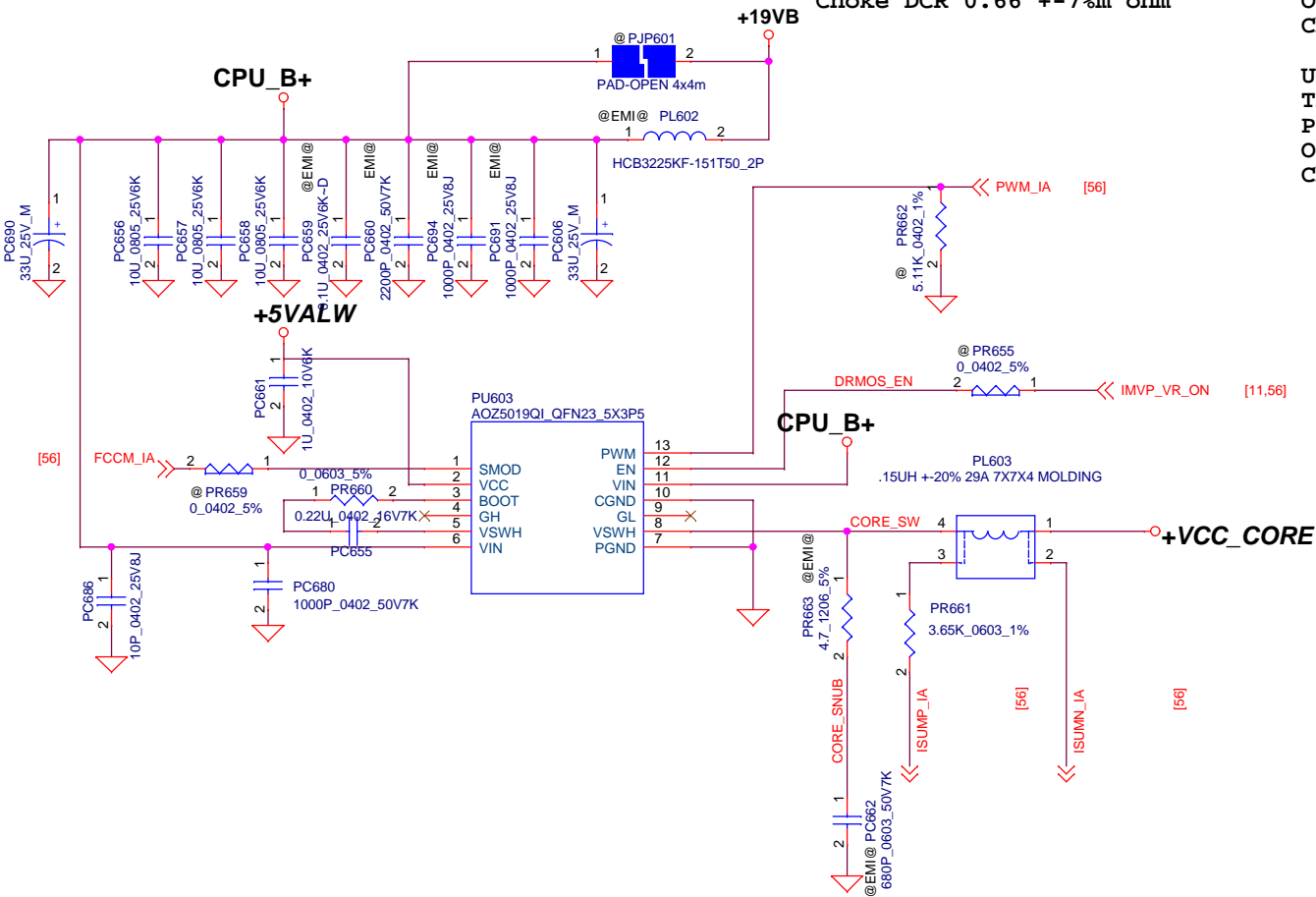
VCC_core
U22 - 15W
Loadline : 2.4m-ohm
U23e - 15W
Loadline : 2.4m-ohm

TDC 21A
Peak Current 29A (KBL : 32A)
OCP current 34A (KBL : 36A)
Choke DCR 0.66 +-7% ohm

VCC_GT
U22 - 15W
Loadline : 3.1m-ohm
U23e - 15W
Loadline : 2m-ohm

U22-15W
TDC 18A
Peak Current 31A
OCP current 37A
Choke DCR 0.66 +-7% ohm

U23e-15W
TDC 36A
Peak Current 64A
OCP current 77A
Choke DCR 0.66 +-7% ohm



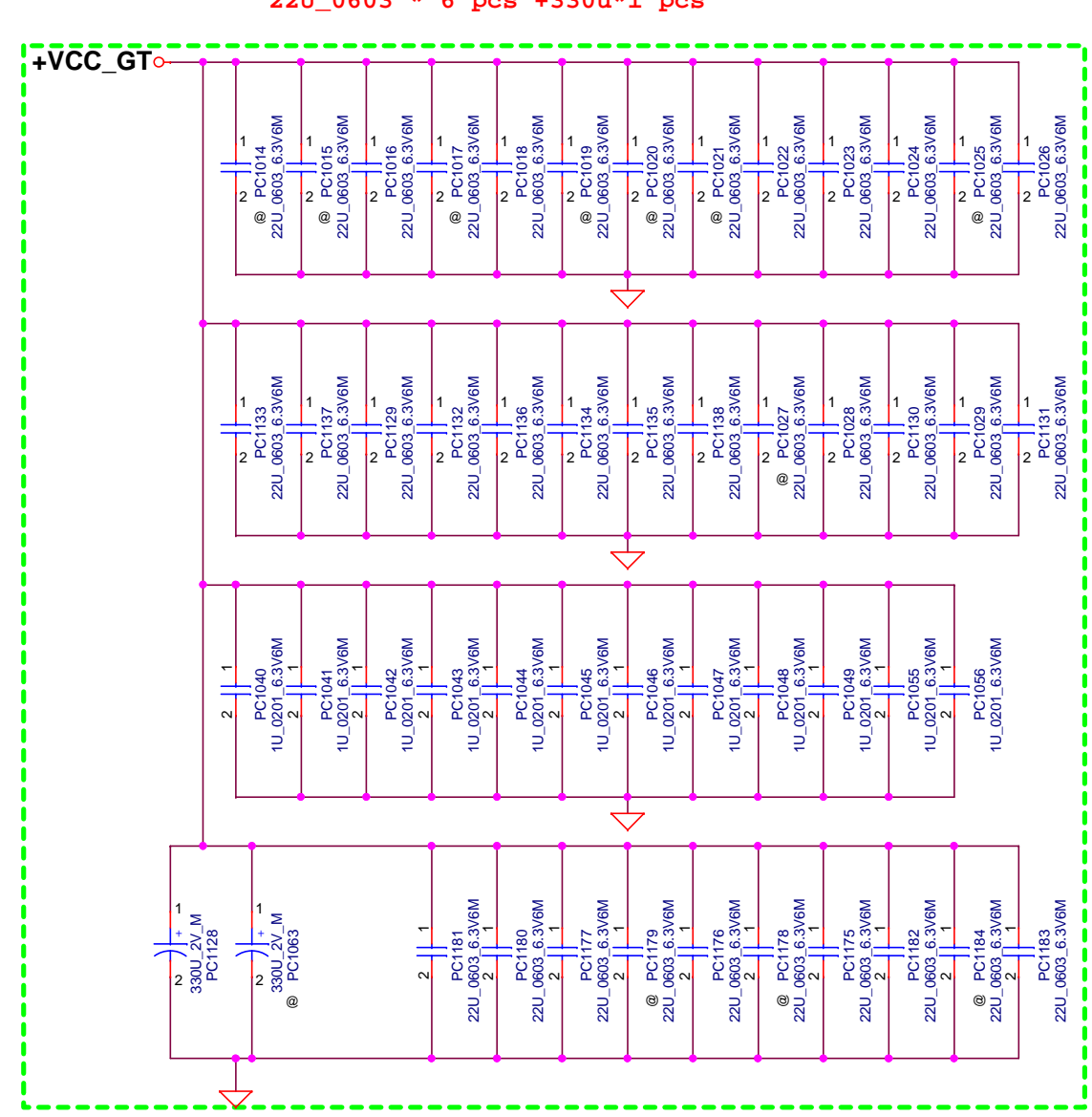
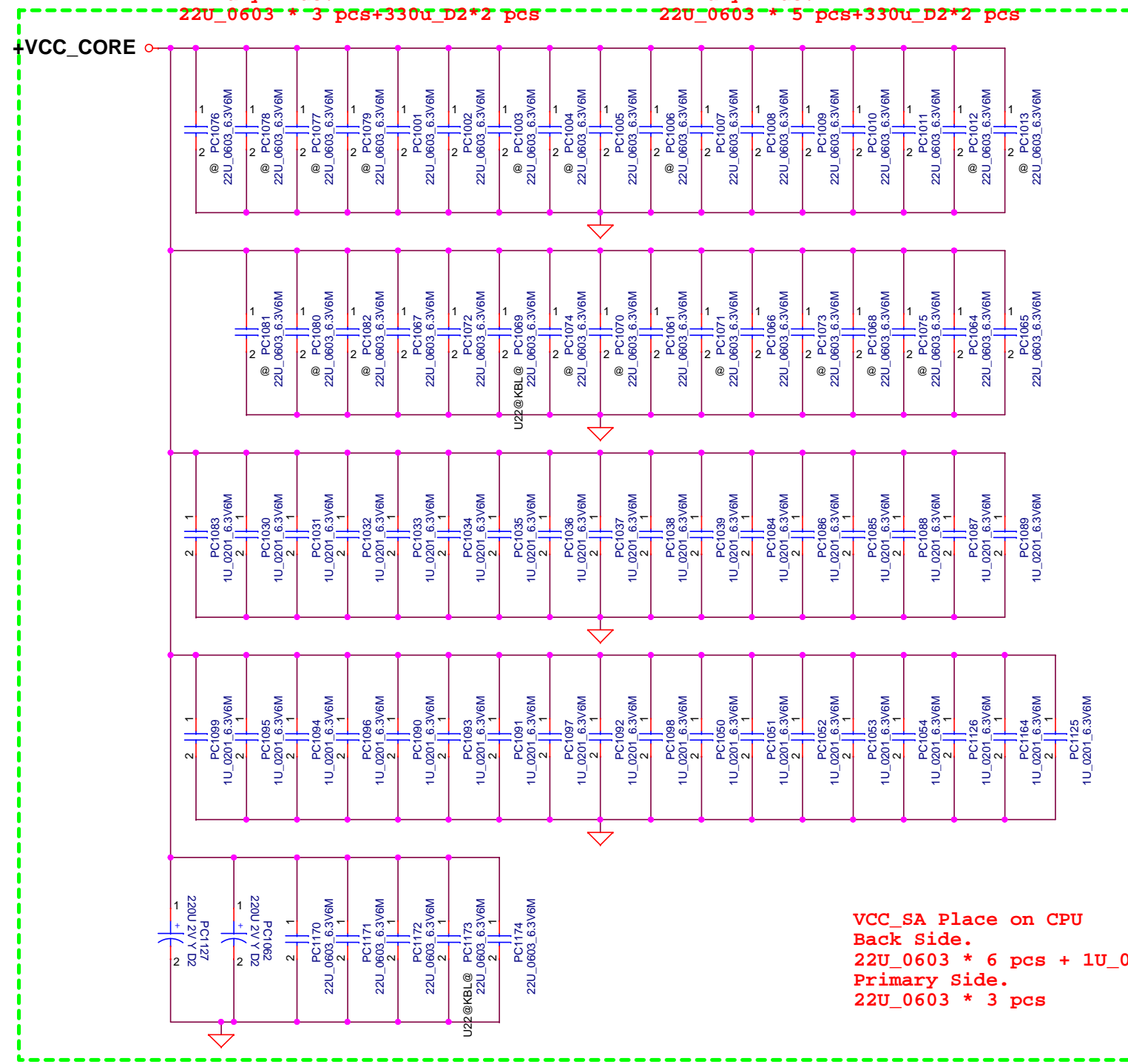
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Issued Date	2015/03/23	Deciphered Date	2014/12/15	PWR +VCC_core and +VCC_GT	
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				Sheet	57 of 61
				Rev	X00

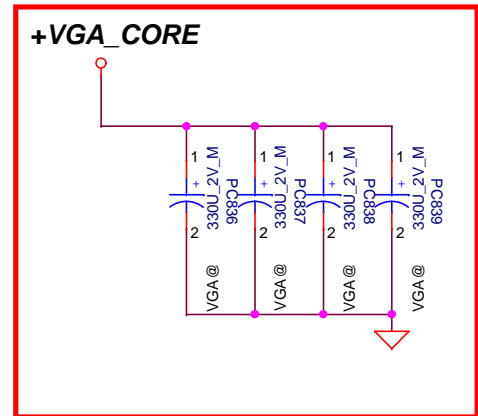
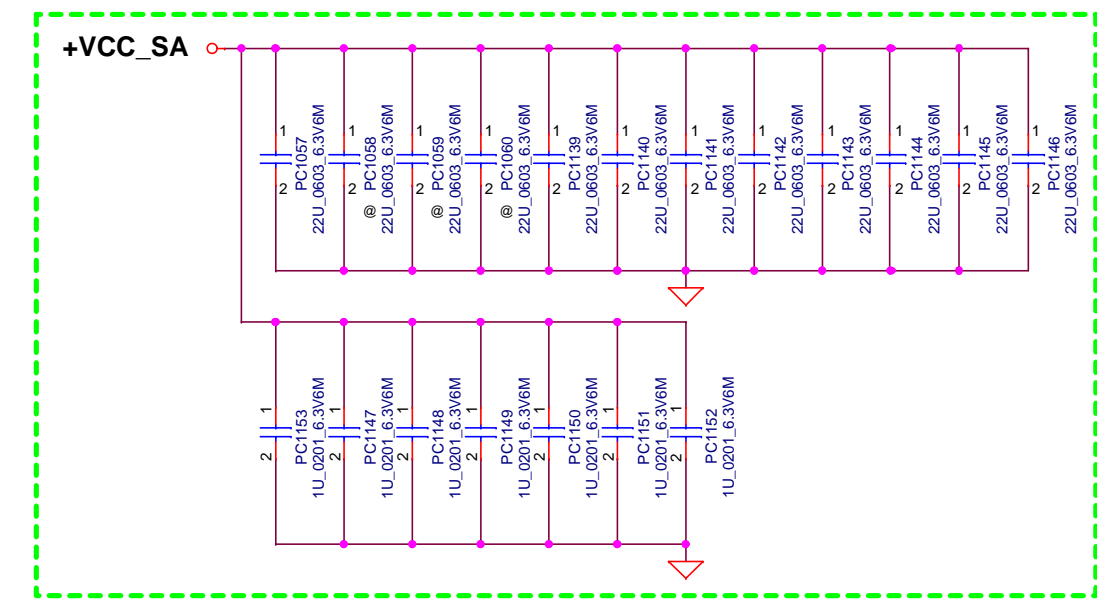
SKL :
VCC_CORE Place on CPU
Back Side.
22U_0603 * 15 pcs +1U_0201*35 pcs
Primary Side.
22U_0603 * 3 pcs+330u_D2*2 pcs

KBL :
VCC_CORE Place on CPU
Back Side.
22U_0603 * 15 pcs +1U_0201*35 pcs
Primary Side.
22U_0603 * 5 pcs+330u_D2*2 pcs

VCC_GT Place on CPU
Back Side.
22U_0603 * 19 pcs +1U_0201*12 pcs
Primary Side.
22U_0603 * 6 pcs +330u*1 pcs

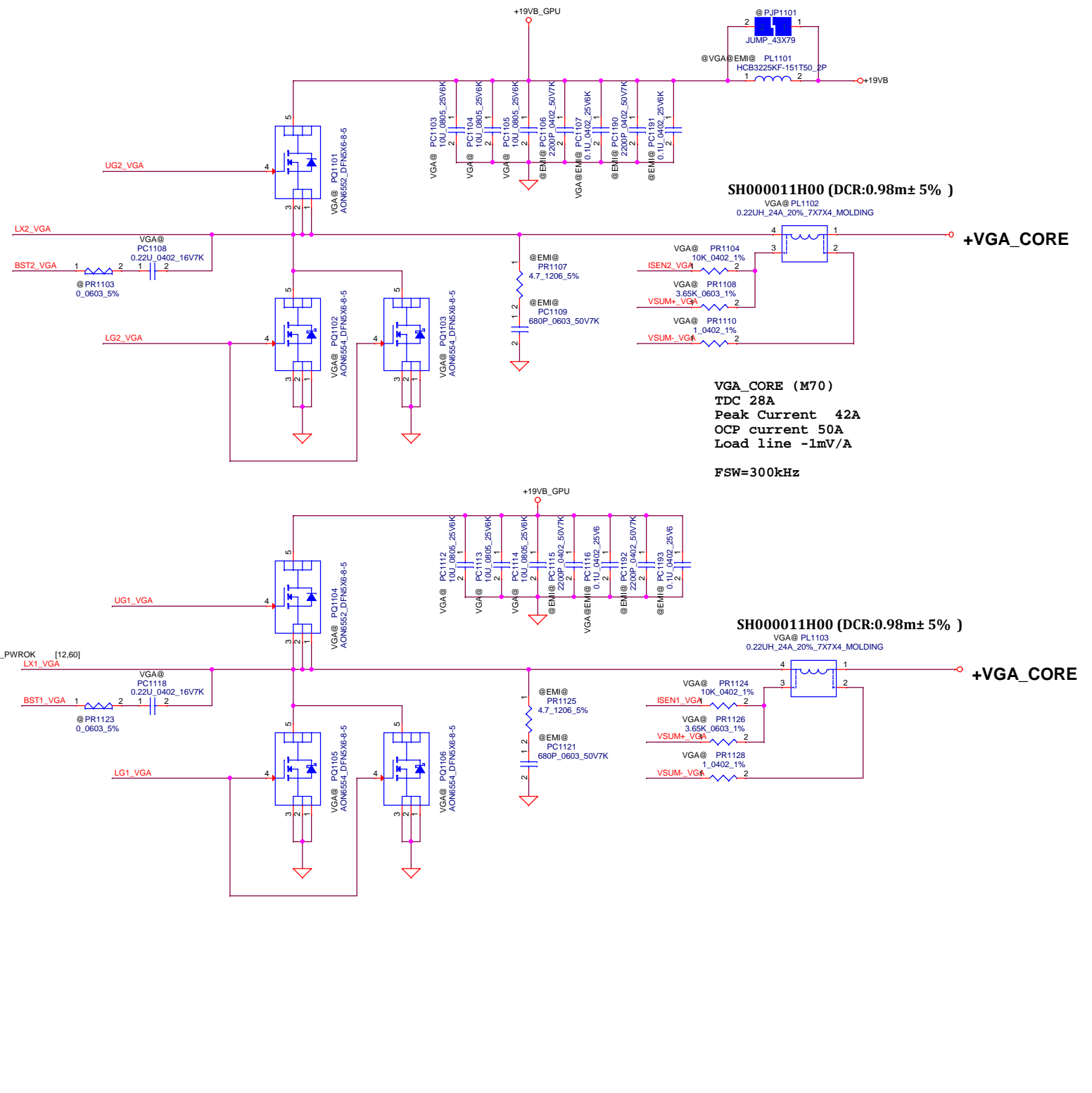


VCC_SA Place on CPU
Back Side.
22U_0603 * 6 pcs + 1U_0201*7 pcs
Primary Side.
22U_0603 * 3 pcs

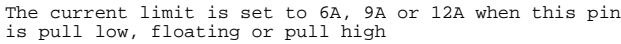


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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/03/23	Deciphered Date	2014/12/15	Title	PWR_VGA_CORE
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OCP setting	ILMT(pin13)
6A	Pull low
9A	Floating
12A	Pull high

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Issued Date		2014/03/31		Deciphered Date		2015/04/30		Title	
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		Size		Document Number					Rev
				LA-D801P					X00
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P51	PWR	20160321	COMPAL	design change charger IC design change	PU706 change to ISL88739 PR732 change to 53.6K PR774 change to 1K PC748 change to 0.1U delete PR727,PC762,PC763,PC776	0.1(X00)
2	P56	PWR	20160321	COMPAL	design change for IA_Core Iccmax 32A	Change the PR640 to 280 Ohm Change the PR648 to 1.5k Change the PR629 to 93.1k	0.1(X00)
3	P58	PWR	20160321	COMPAL	design change	delete PC1003,PC1004,PC1006,PC1012,PC1013,PC1014,PC1015,PC1017,PC1019,PC1020,PC1021,PC1025,PC1027,PC1058,PC1059,PC1060,PC1068,PC1070,PC1071,PC1073,PC1074,PC1075,PC1076,PC1077,PC1078,PC1079,PC1080,PC1081,PC1082 add PC1170,PC1171,PC1172,PC1173,PC1174,PC1175,PC1176,PC1177,PC1180,PC1181,PC1182,PC1183	0.1(X00)
4	P50	PWR	20160504	COMPAL	Reserve Erp lot6	Reserve PR2,PR5 ,PR7,PR10,PQ1	0.3(X02)
5	P51	PWR	20160504	COMPAL	PQ740 damage issue	Change PQ740 to SB00000SY00 (MDU1512R)	0.3(X02)
6	P51	PWR	20160504	COMPAL	EMI solution	Change to SE068102J80 (1000P) Location : PC780,PC781,PC100,PC131,PC115,PC133,PC230,PC231,PC694,PC691,PC692,PC693,PC1420,PC1421	0.3(X02)
7	P51	PWR	20160614	COMPAL	Change SOT23-6P to SOT23-3P	change PQ709 to SB00000ST00 (PQ709,PQ712)	1.0(A00)
8	P51	PWR	20160614	COMPAL	Add pull high resistance	Add PR781	1.0(A00)

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				Date:	Tuesday, June 21, 2016
				Sheet	61 of 61